

FIG. 2 (PRIOR ART)

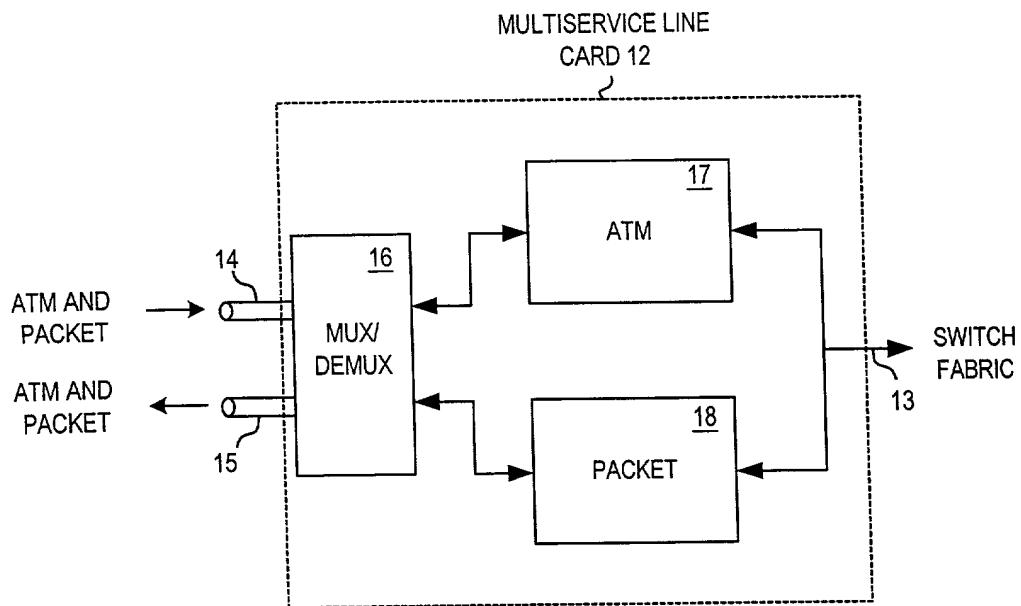


FIG. 3

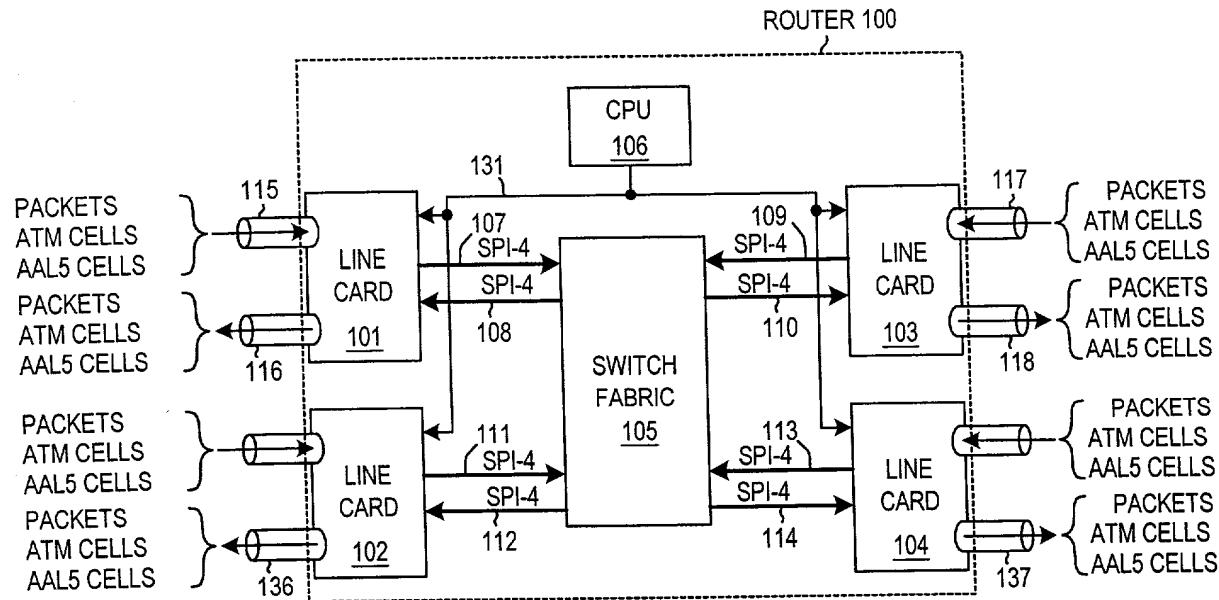


FIG. 4

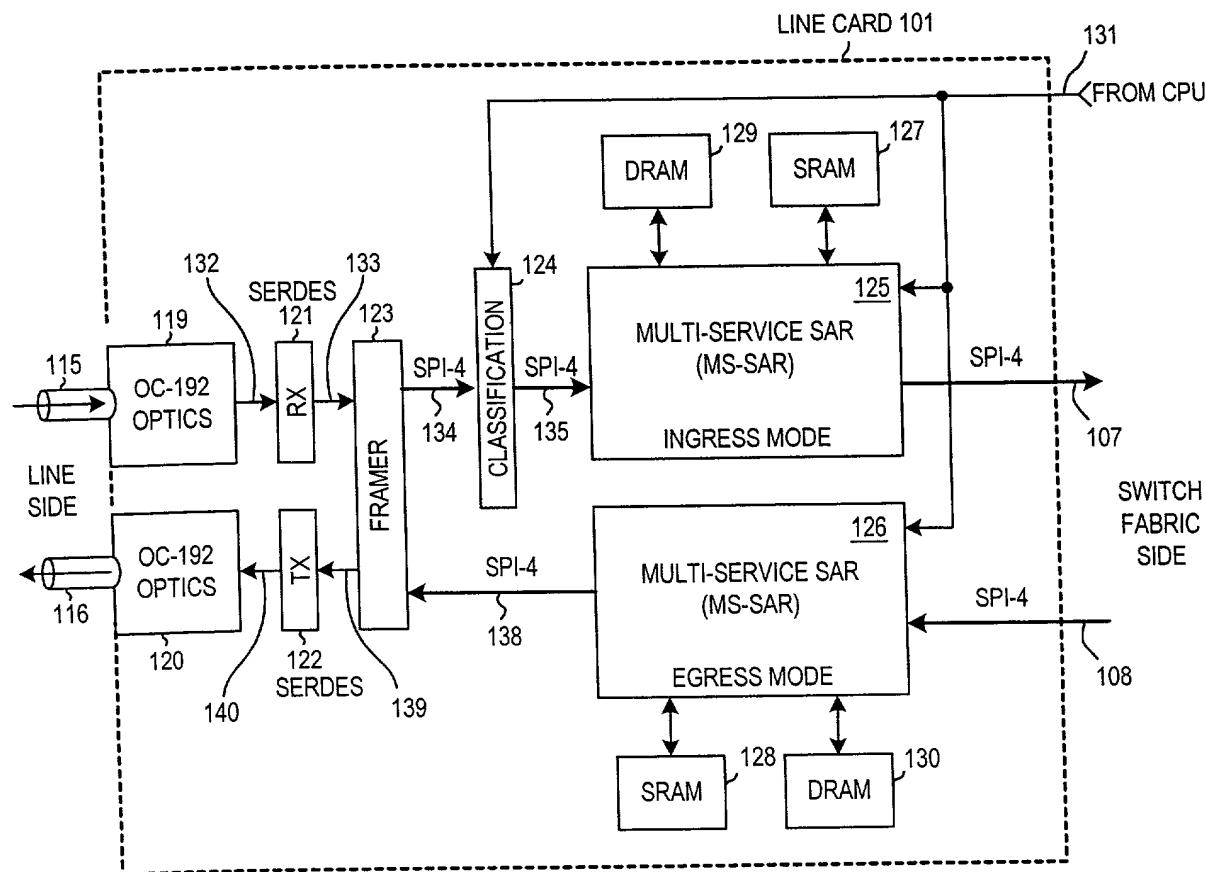


FIG. 5

SWITCH FABRIC	APPLICATION TYPE	INGRESS APPL TYPE	EGRESS APPL TYPE
CELL	ATM => ATM	0	8
	ATM => MPLS PACKET	1	9
	MPLS PACKET => ATM	2	10
	MPLS PACKET => MPLS PACKET	3	11
PACKET	ATM => PACKET	4	14
	PACKET => ATM	6	12
	AAL5 => PACKET	5	14
	PACKET => AAL5	6	13
	PACKET => PACKET	6	14

APPLICATION TYPES

FIG. 6

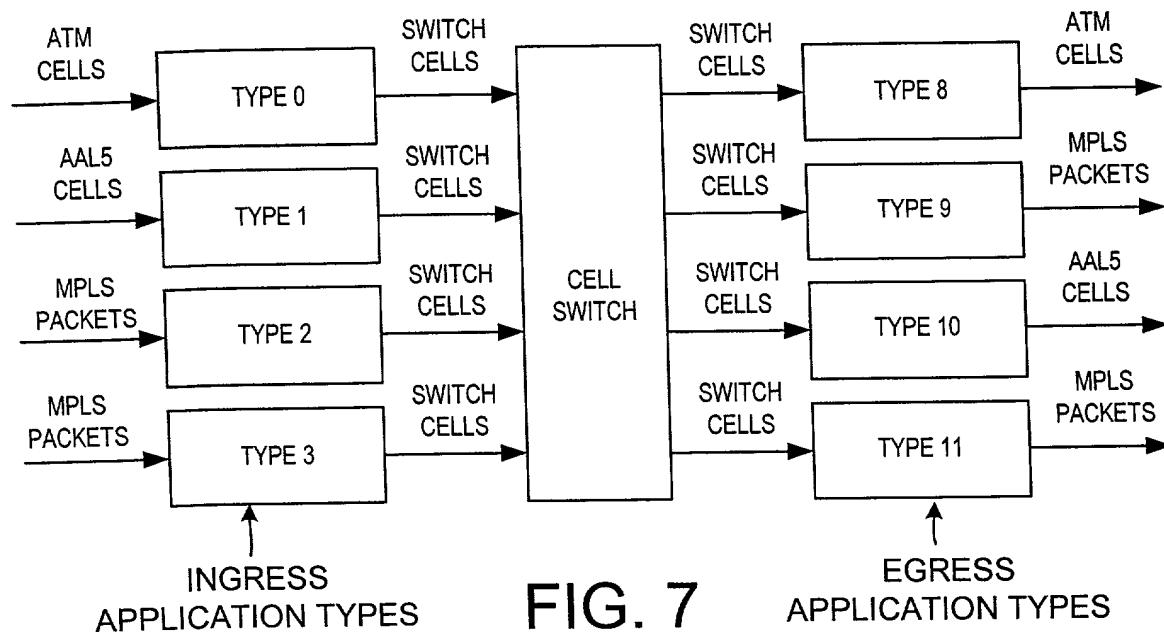


FIG. 7

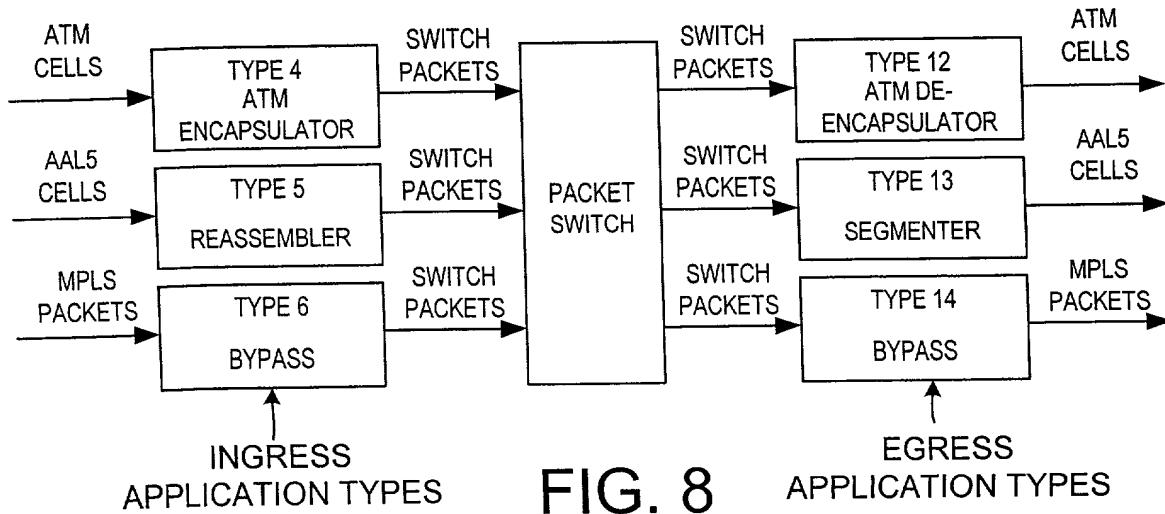


FIG. 8

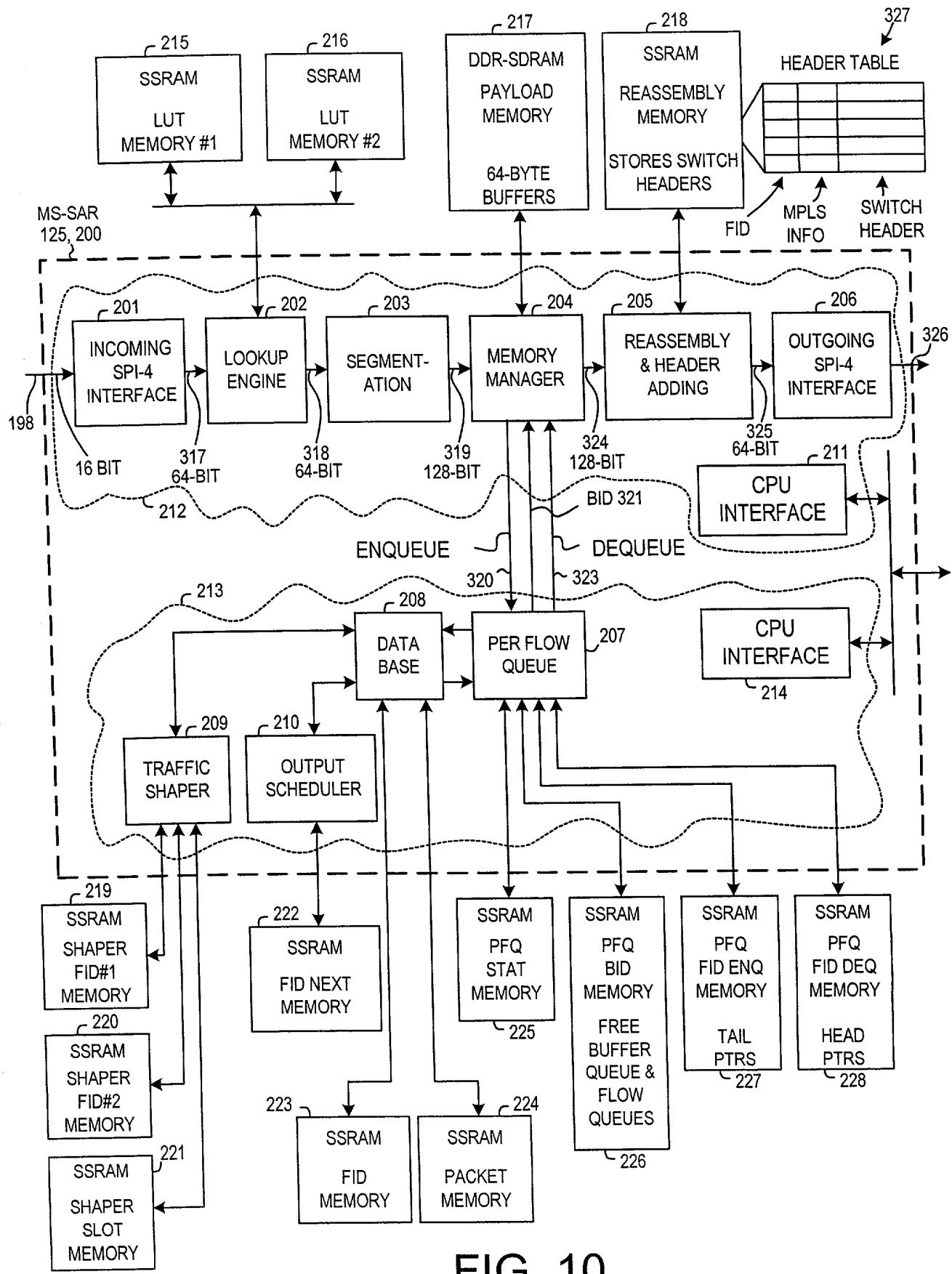


FIG. 10

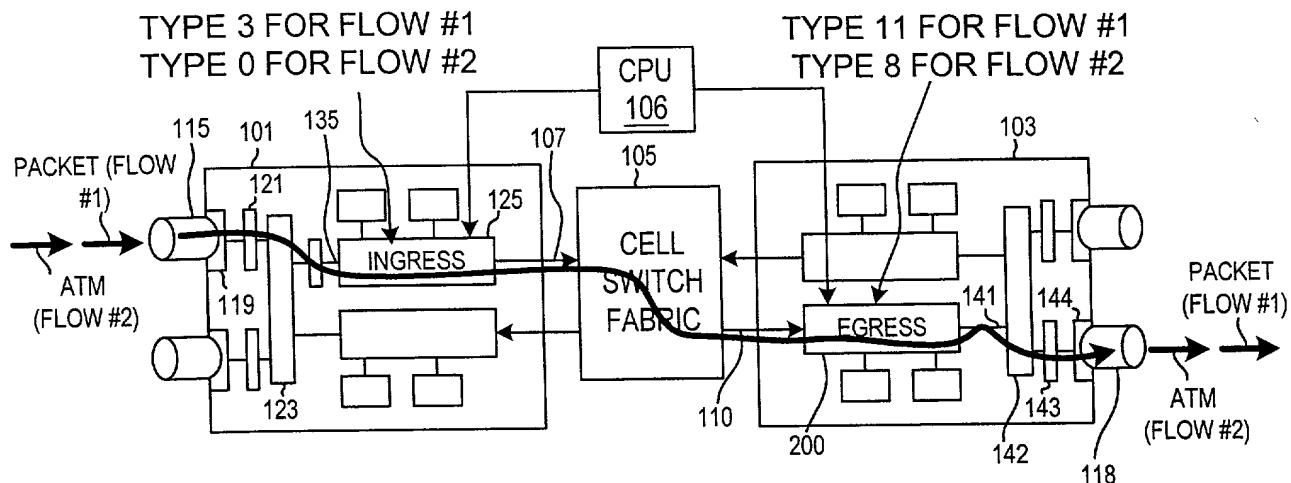


FIG. 9

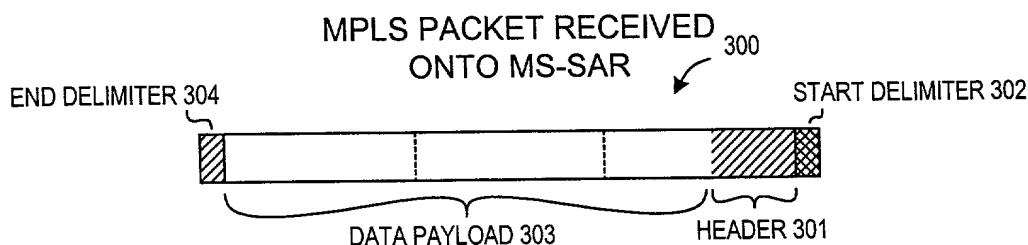


FIG. 11

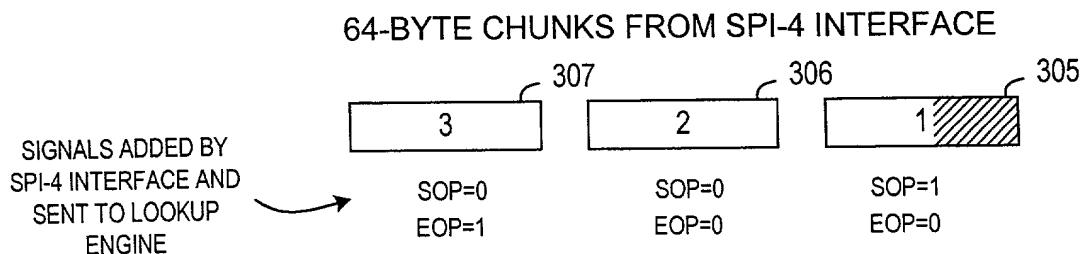
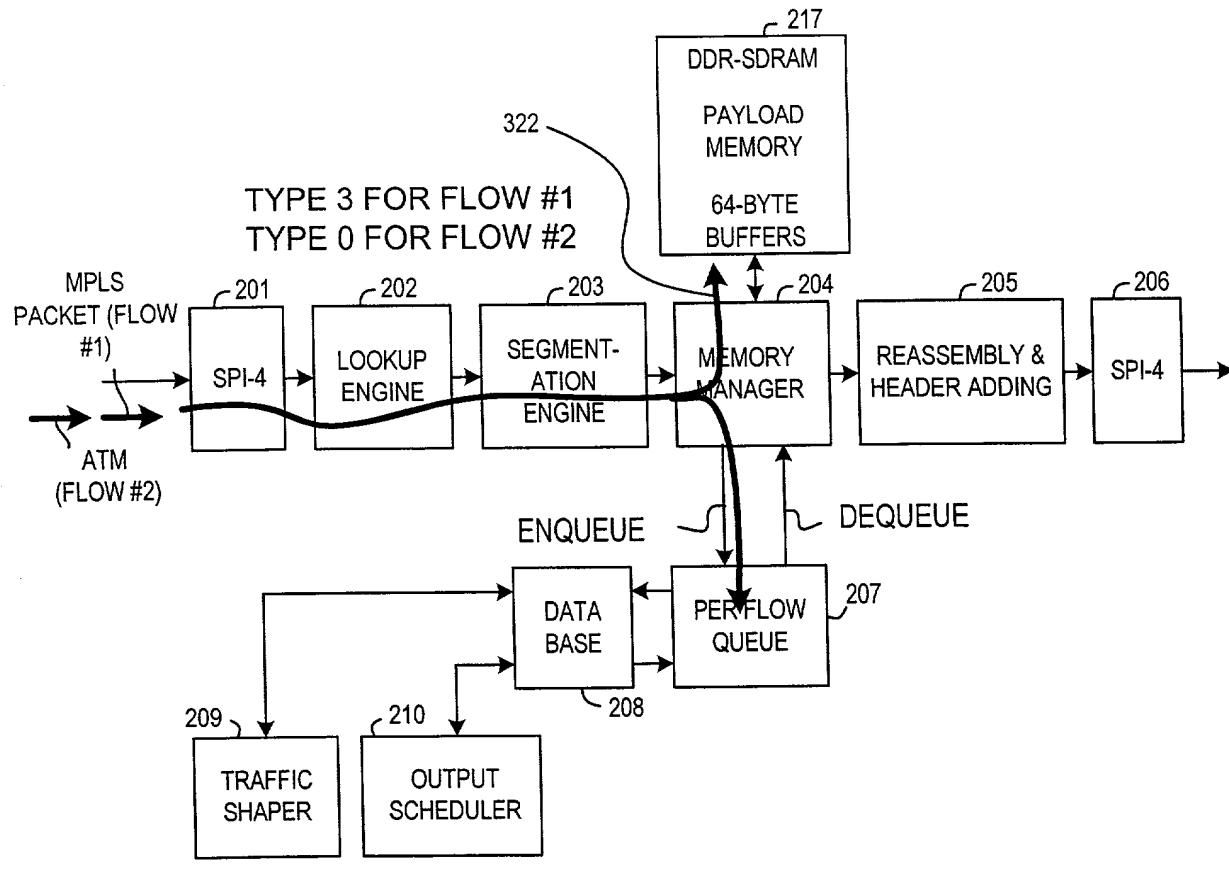


FIG. 12



INGRESS MODE

FIG. 13

PORT TABLE IN LOOKUP BLOCK

64 LOGICAL INPUT PORTS	1		10000	0
	45		10000	0
	INPUT PORT NUMBER		NUMBER OF BYTES OF SWITCH HEADER (USED BY EGRESS)	TRAFFIC TYPE (USED BY INGRESS)

FIG. 14

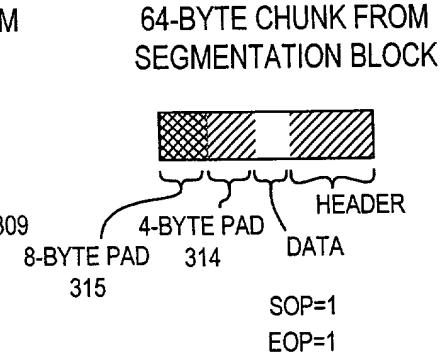
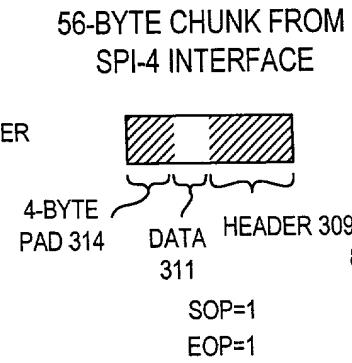
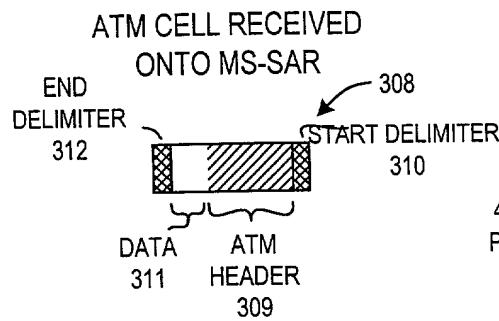
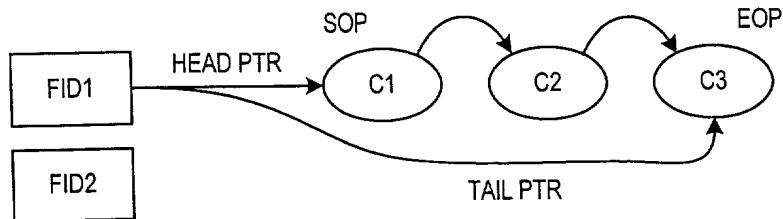
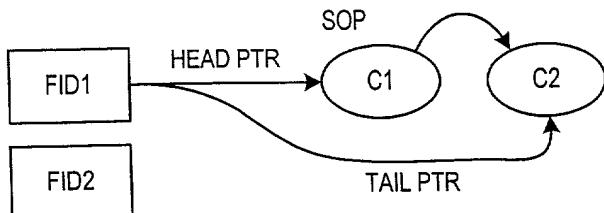
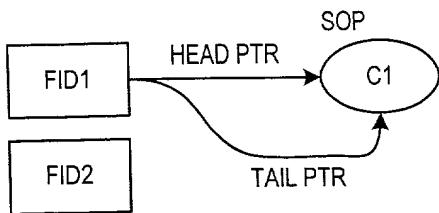


FIG. 20

FIG. 21

FIG. 22

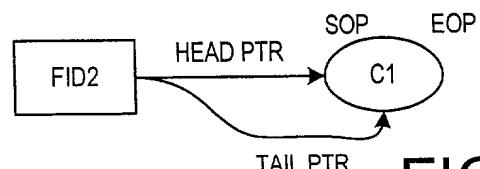
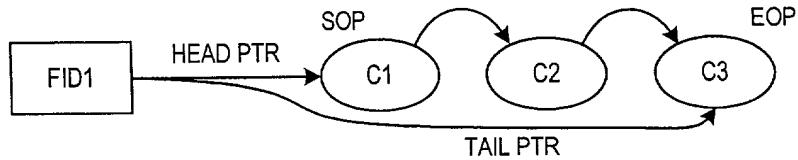


FIG. 23

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID HEAD	23	22:0	H	HEAD POINTER. FIRST BUFFER TO BE ENQUEUED, AND FIRST BUFFER TO BE DEQUEUED. IF NULL, THE QUEUE IS EMPTY.
HD EOP PKT	1	23	H	IF SET, THE HEAD BID IS THE EOP.
HD SOP PKT	1	23	H	IF SET, THE HEAD BID IS THE SOP.
HD EFCI	1	25	H	EFCI BIT.
CLP	1	26	H	CLP BIT. CAN BE MODIFIED BY DBS.
OAM	1	27	H	OAM BIT.
SPARE	1	28	H	
CLASS	3	31:29	H	CLASS OF FID.
FID TYPE	4	35:32	H	APPLICATION TYPE INDICATES THE PROCESSING THAT THE MS-SAR WILL TAKE ON THIS FLOW. WILL BE SENT TO MEMORY MANAGER. TYPE IS WRITTEN WITH THE HEAD POINTER.

FID DEQUEUE MEMORY LOCATION

FIG. 16

00000000000000000000000000000000

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID TAIL	23	22:0	H	TAIL POINTER. LAST BUFFER TO BE ENQUEUED, AND LAST BUFFER TO BE DEQUEUED. IF NULL, THE QUEUE IS EMPTY.
BID PRV PKT TAIL	23	45:23	H	BID OF PREVIOUS PACKET'S TAIL BID. SAVED ON EOP.
TTL	1	46	H	WHEN 1, DISCARD AND DEACTIVATE THE FID.
OUTPUT PORT#	7	53:47	S	OUTPUT PORT NUMBER THAT THE FID WILL BE TRANSMITTED ON.
Q SIZE	18	71:54	H	SIZE OF THE QUEUE IN BIDS. INCREMENTED ON ENQUEUE. DECREMENTED ON EVERY DEQUEUE OPERATION.

FIRST FID ENQUEUE MEMORY LOCATION

FIG. 17

10/45

NAME	NO BITS	RANGE	WR	DESCRIPTION
VALID	1	0	S	IF SET, THEN ENQUEUE. IF NOT, THEN SETUP CONNECTION COMMAND AS NEEDED BEFORE ENQUEUE STARTS.
SPARE	8	8:1		
DROP UNTIL SOP	1	9	H	DROP UNTIL THE NEXT SOP.
SEL DROP COUNT ER	1	10	H	SEL THE COUNT FOR DROPPING.
SPARE	2	12:11		
CURRENT TAIL PKT CELL CNT	11	23:13	H	REPRESENTS THE NUMBER OF CELLS IN THE TAIL PACKET THAT IS BEING ENQUEUED.
SPARE	2	25:24		
ENQ NOT DISCARD RED PKT COUNT	16	41:26	H	THE NUMBER OF NOT DISCARDED PACKETS THAT HAVE ARRIVED SINCE LAST RED DISCARD. IT IS RESET ON THE NEXT RED DISCARD.
SPARE	2	43:42		
AVG	18	61:44	H	THE AVE SIZE OF THE QUEUE.

SECOND FID ENQUEUE MEMORY LOCATION

FIG. 18

NAME	NO BITS	RANGE	WR	DESCRIPTION
BID LINK	23	22:0	H	BID OF THE NEXT BUFFER IN FID QUEUE. ALSO CAN BE A BID LINKED ON THE FREE BUFFER QUEUE.
EOP PKT	1	23	H	END OF PACKET FOR THIS BID BID. EOP BELONGS TO THE BID LINK.
SOP PKT	1	24	H	START OF PACKET FOR THE CORRESPONDING BID. SOP BELONGS TO THE BID LINK.
EFCI	1	25	H	EFCI PASS THROUGH BIT.
OAM	1	26	H	OAM BIT.
CLP	1	27	H	CLP
SPARE	8	35:28		

BID MEMORY LOCATION

FIG. 19

PORT CALENDAR IN REASSEMBLY BLOCK

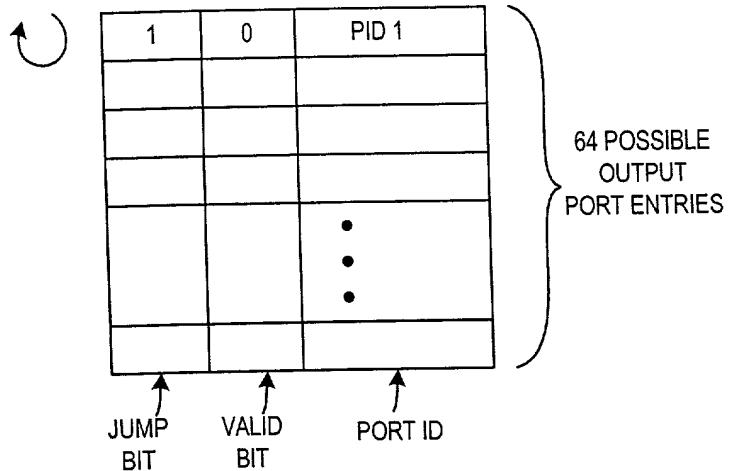


FIG. 24

64 BITS

10000000	•	•	•	000
----------	---	---	---	-----

PORT EMPTY REGISTER

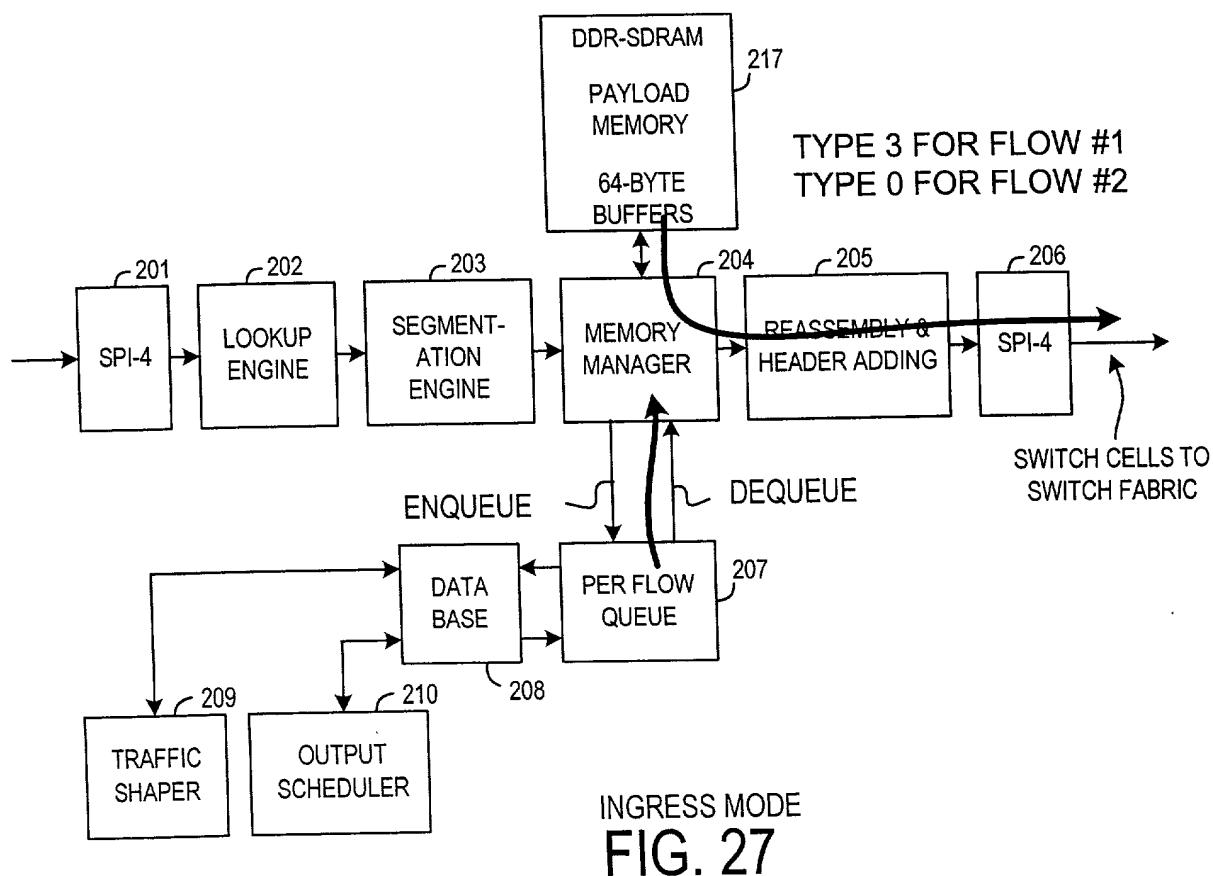
FIG. 25

64 BITS

10000000	•	•	•	000
----------	---	---	---	-----

PORT FULL REGISTER

FIG. 26



12/45

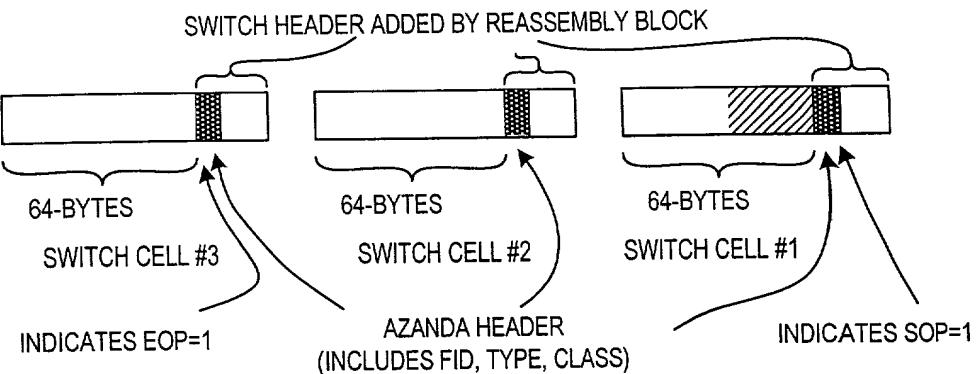


FIG. 28

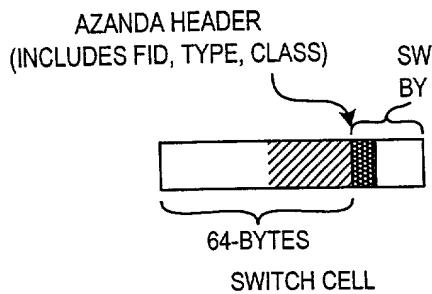


FIG. 29

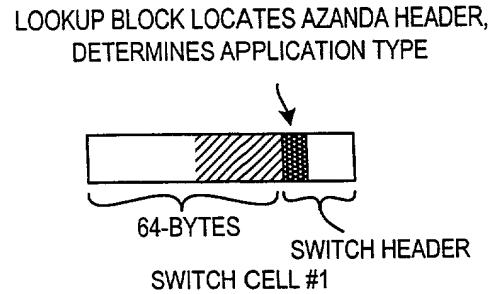


FIG. 31

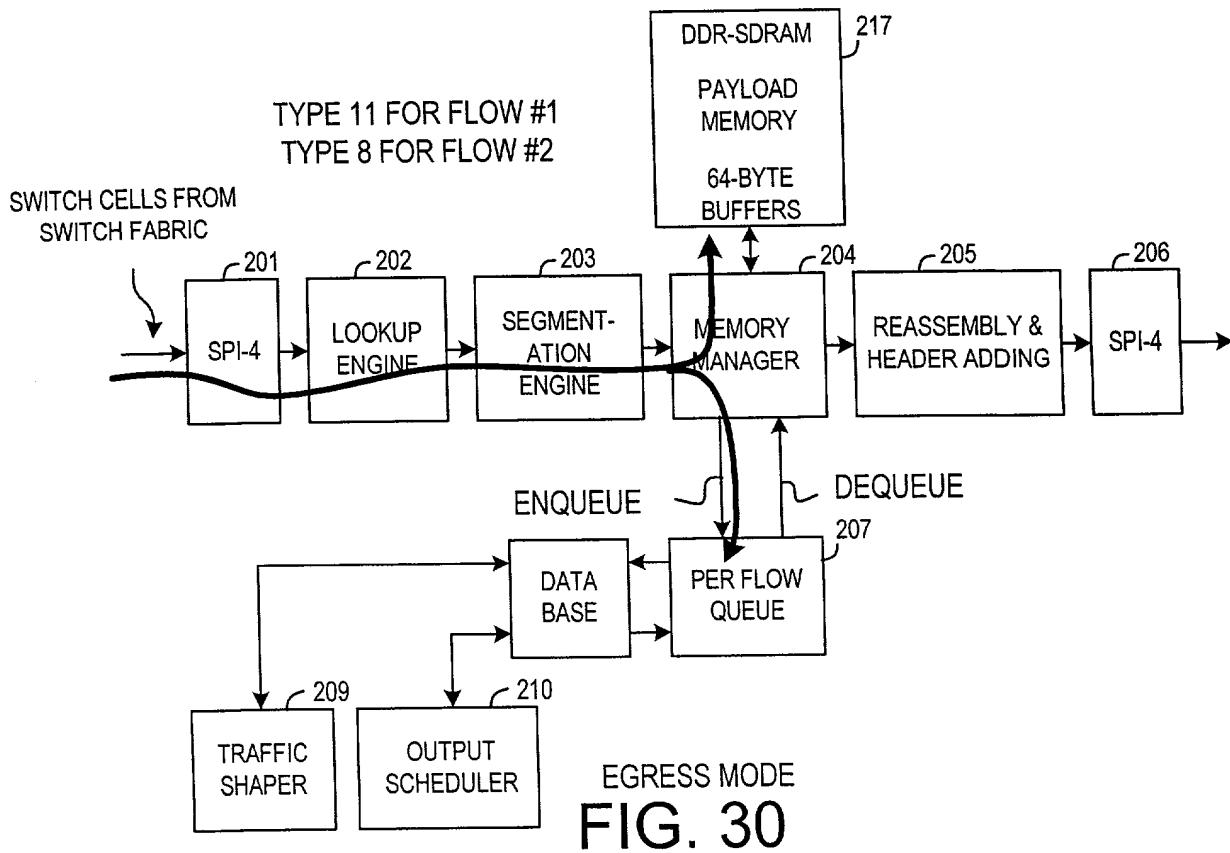
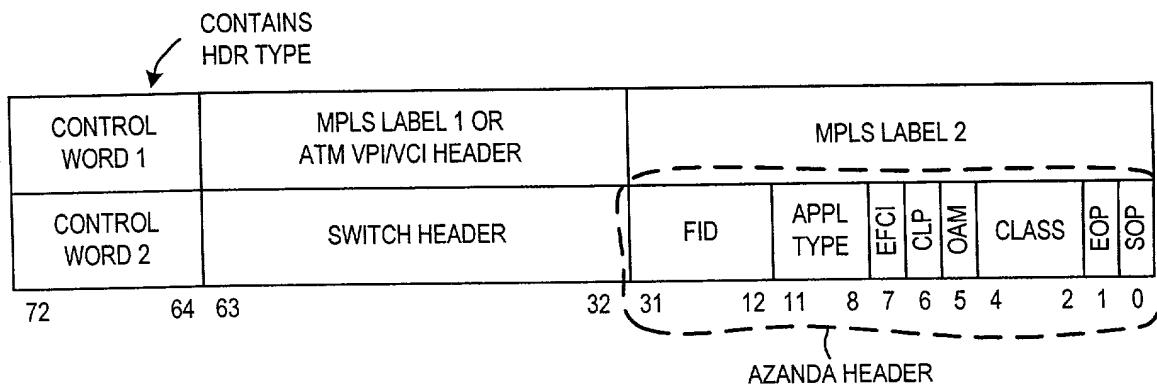
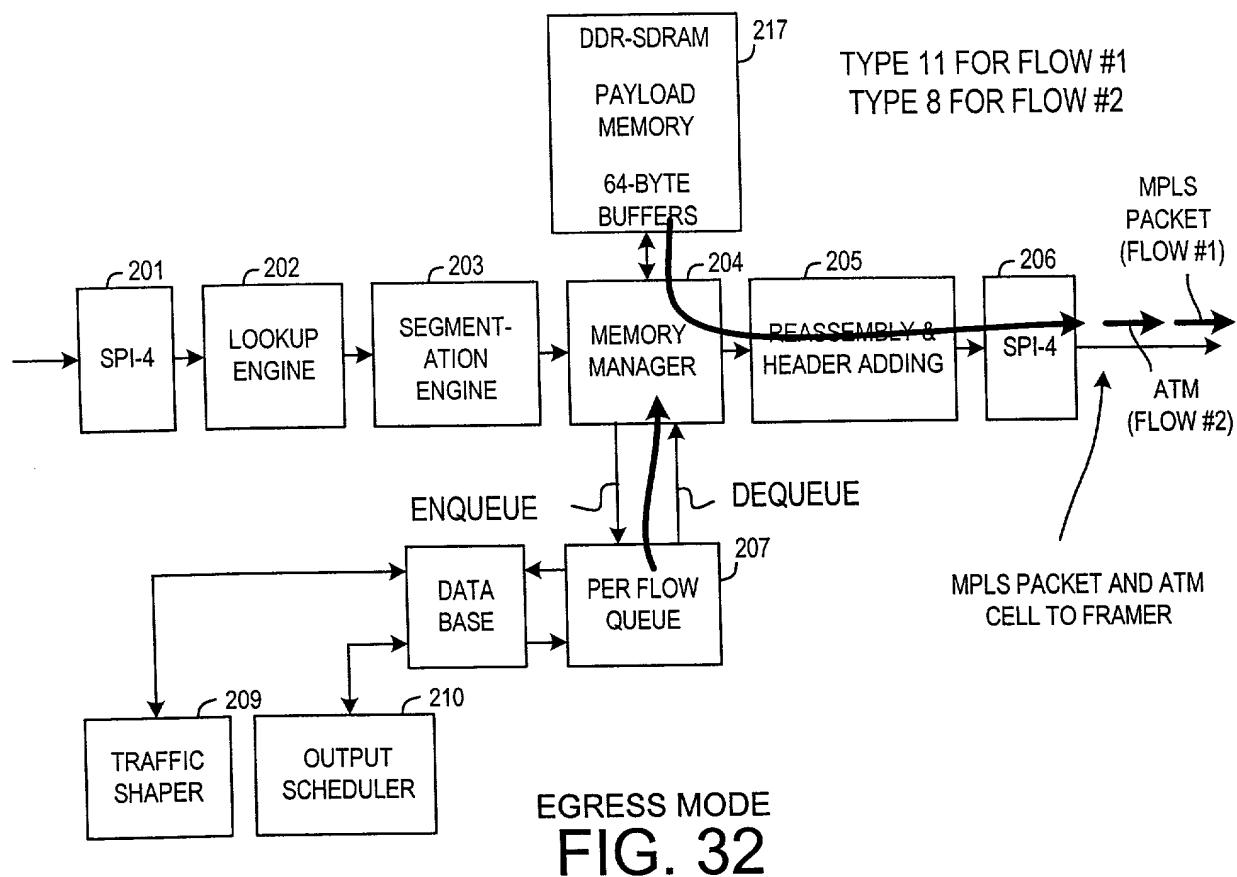


FIG. 30



FORMAT OF ONE FID ENTRY
IN HEADER TABLE

FIG. 33

64-BYTE CHUNKS FROM REASSEMBLY TO SPI-4

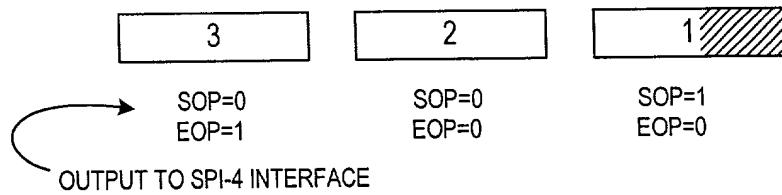


FIG. 34

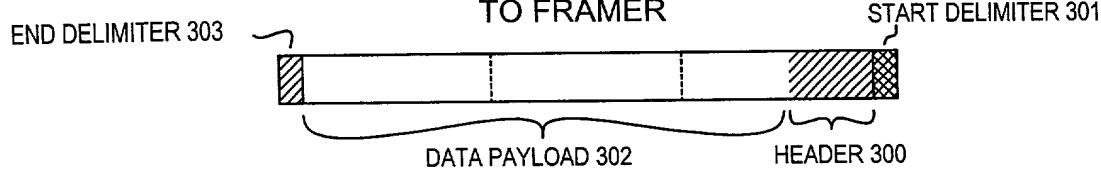
MPLS PACKET OUTPUT
TO FRAMER

FIG. 35

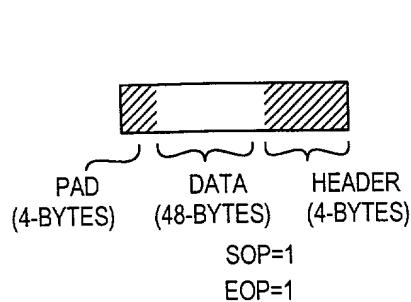
56-BYTE CHUNK FROM
REASSEMBLY BLOCK

FIG. 36

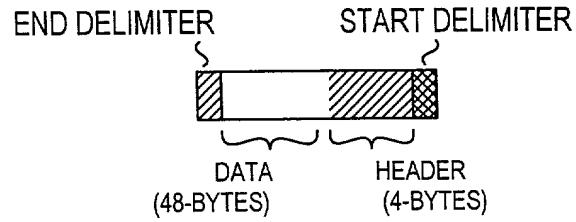
ATM CELL AS OUTPUT
FROM SPI-4 INTERFACE

FIG. 37

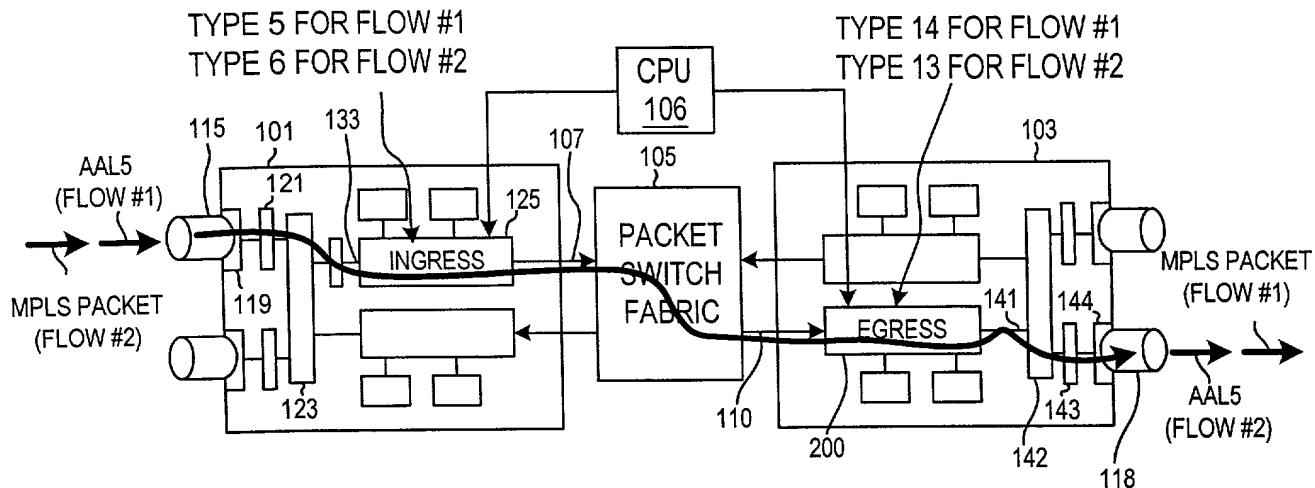


FIG. 38

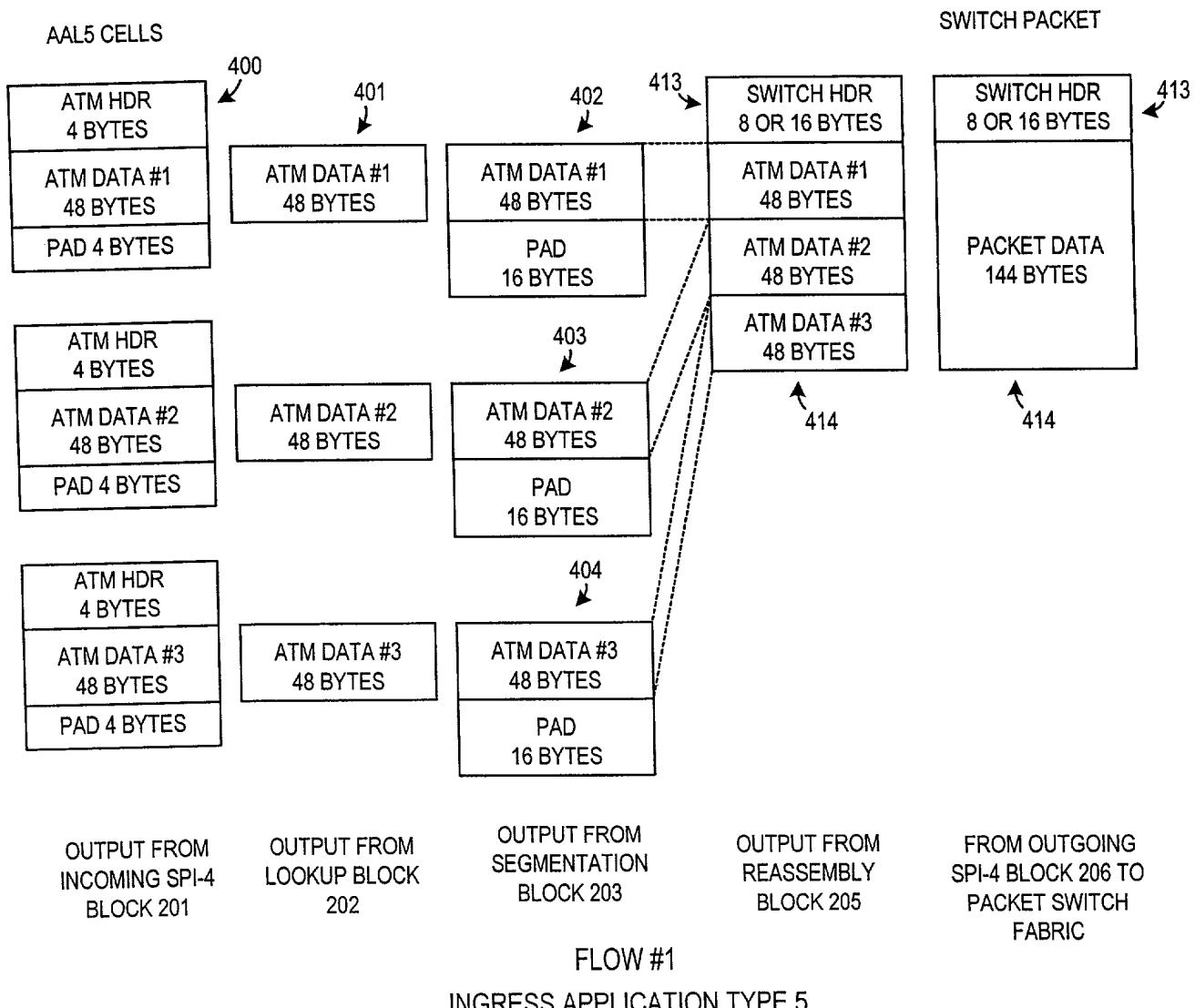
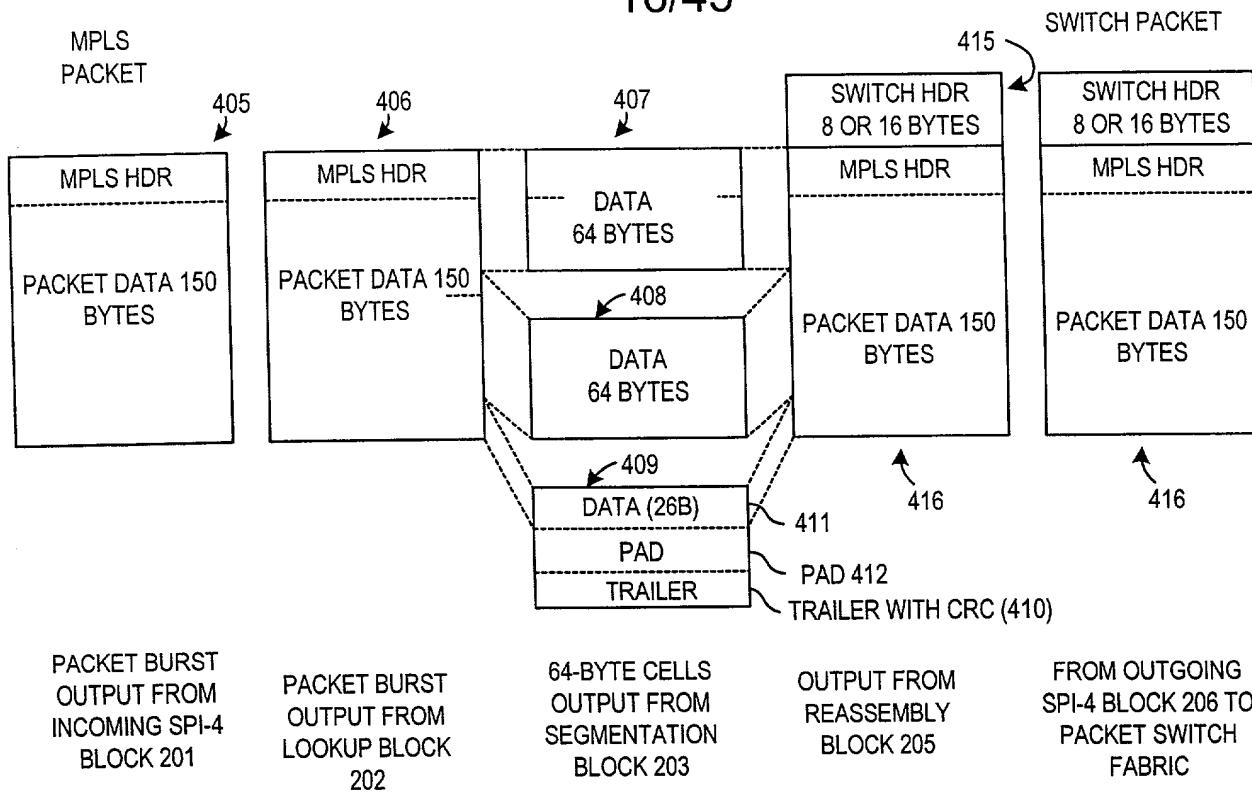


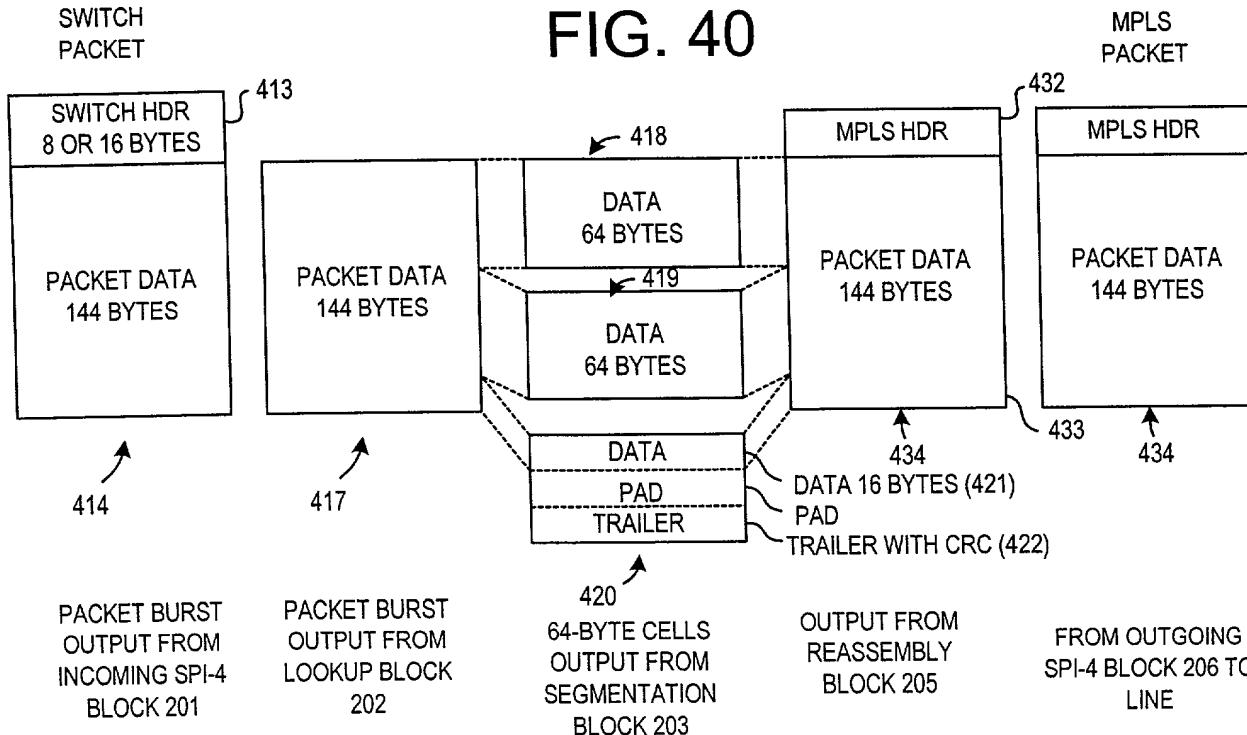
FIG. 39

16/45



FLOW #2

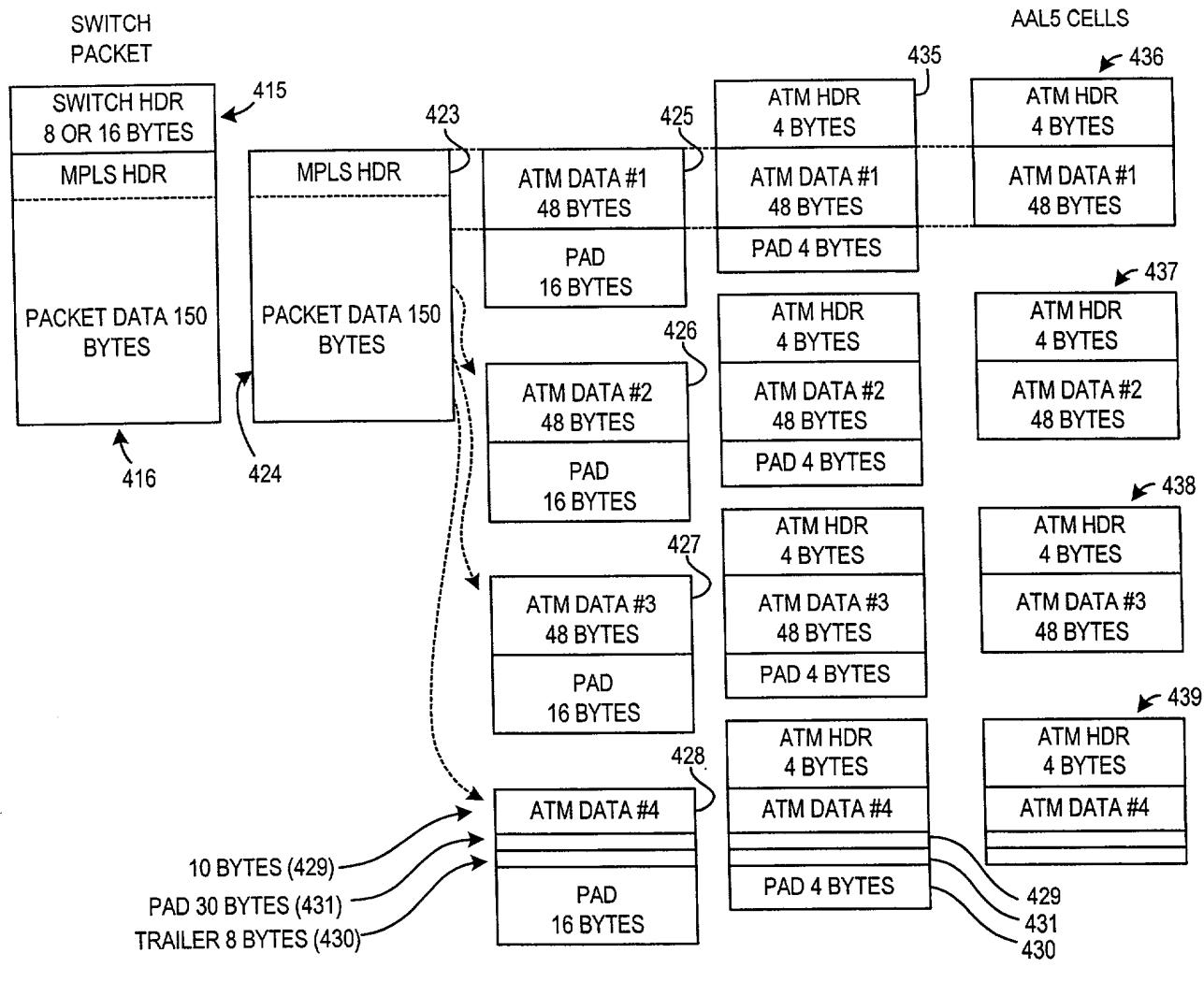
INGRESS APPLICATION TYPE 6

FIG. 40

FLOW #1

EGRESS APPLICATION TYPE 14

FIG. 41



PACKET BURST
OUTPUT FROM
INCOMING SPI-4
BLOCK 201

PACKET BURST
OUTPUT FROM
LOOKUP BLOCK
202

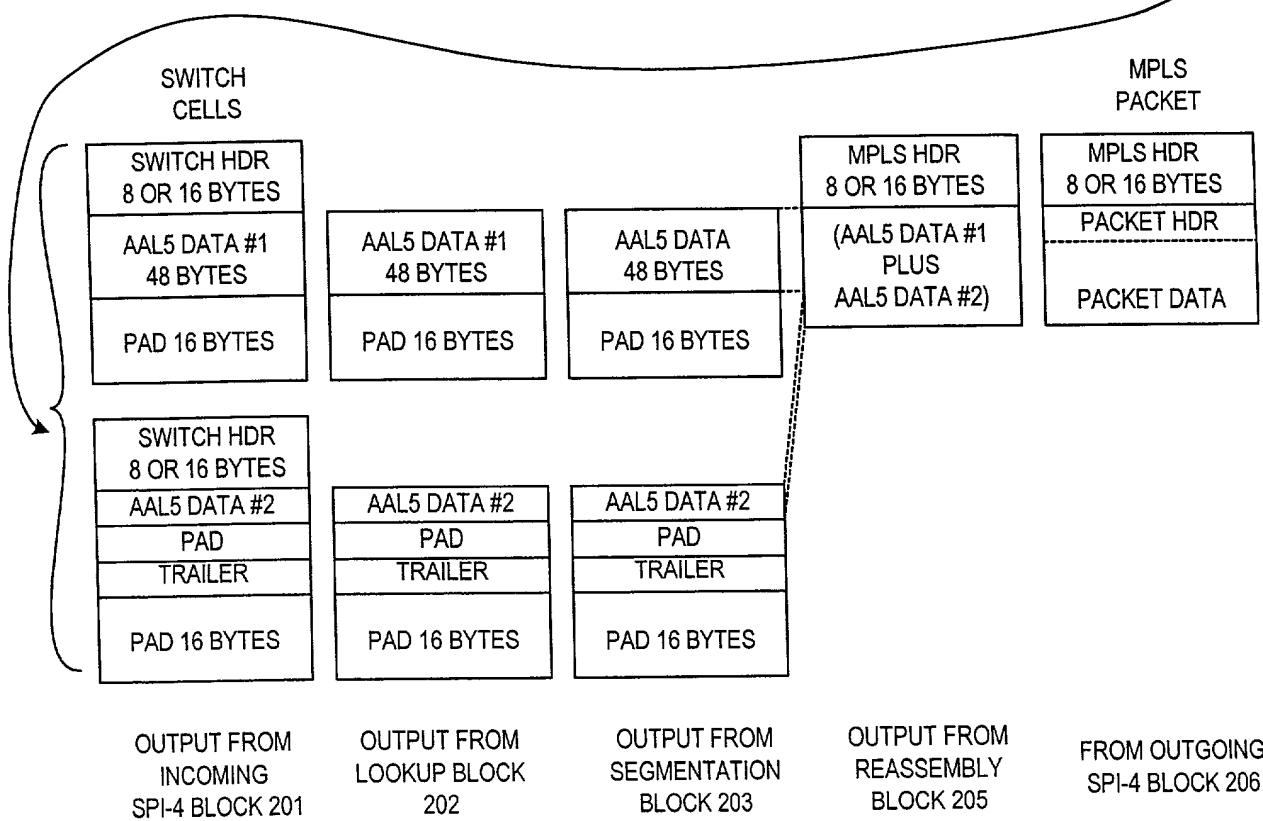
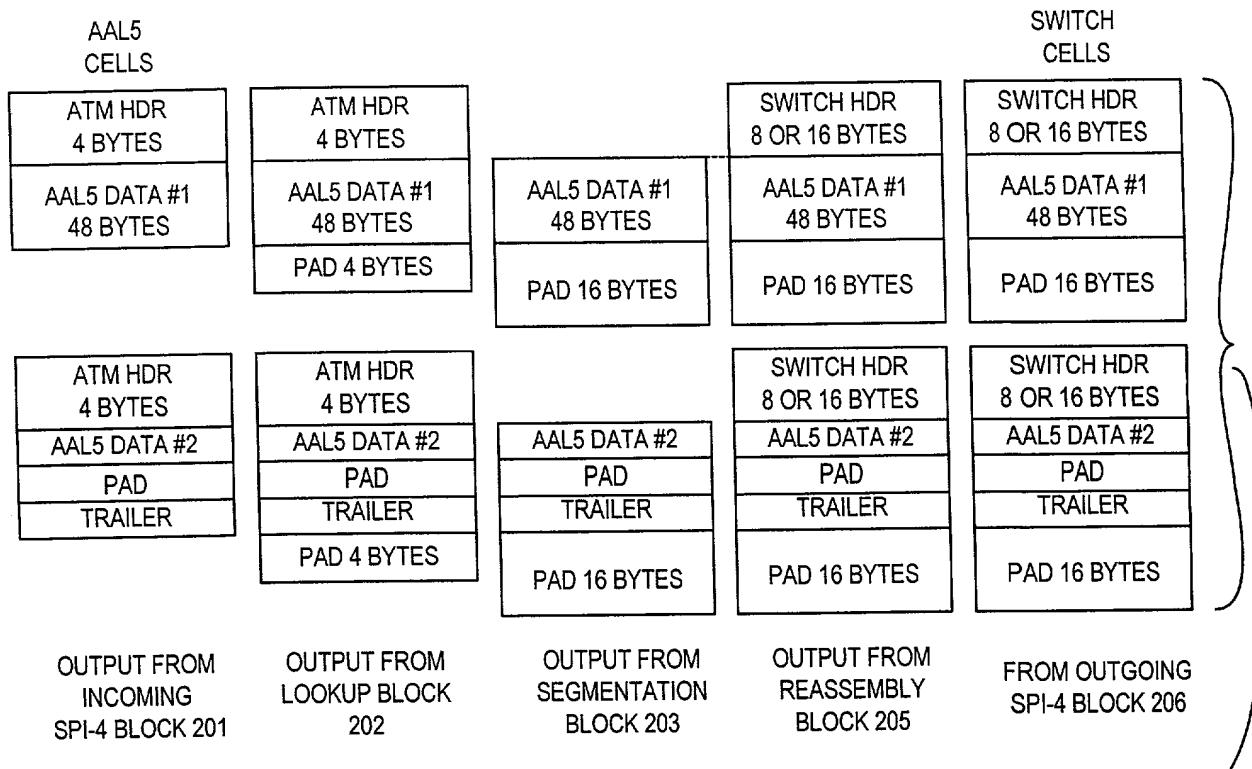
64-BYTE CELLS
OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206 TO
LINE

FLOW #2
EGRESS APPLICATION TYPE 13

FIG. 42



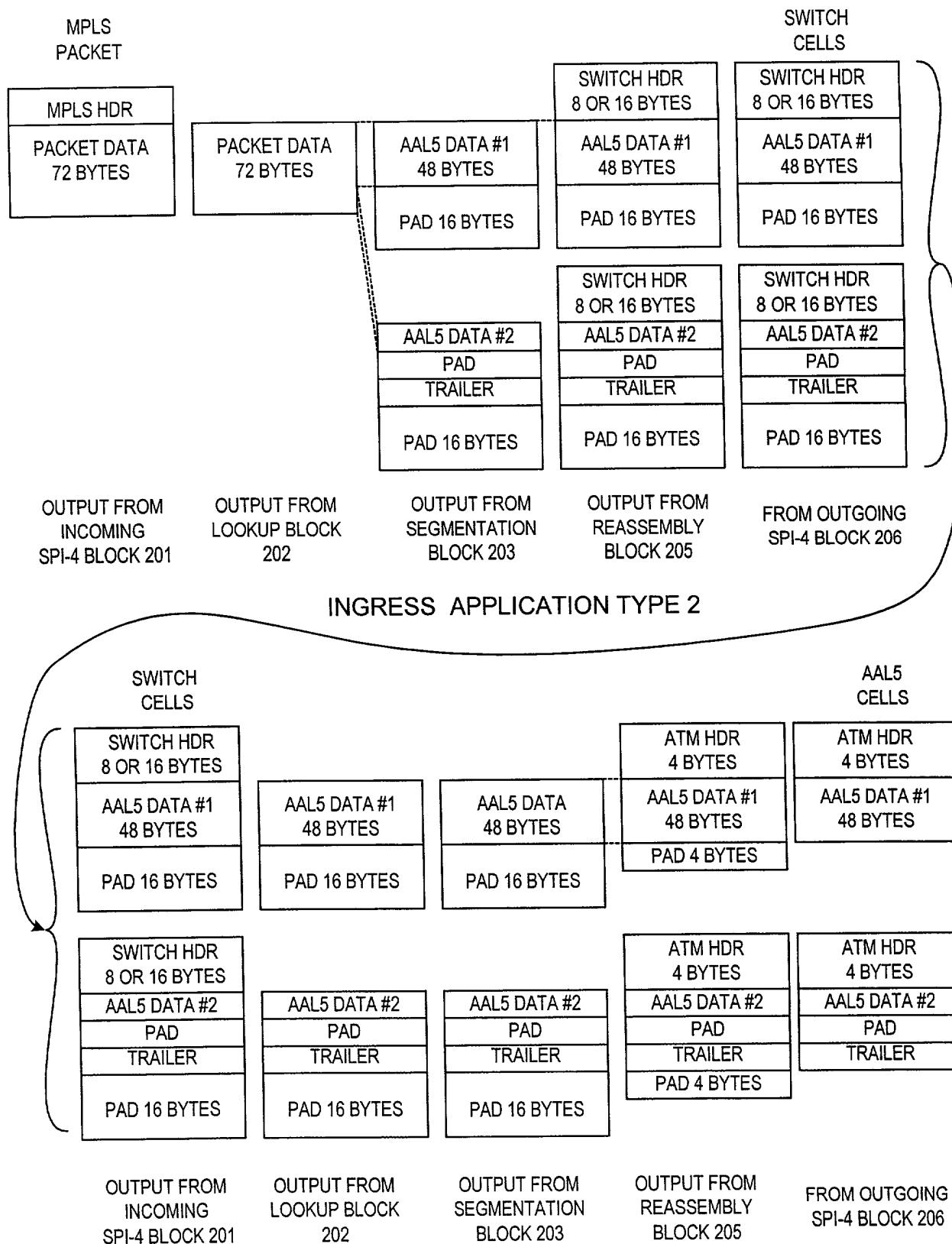
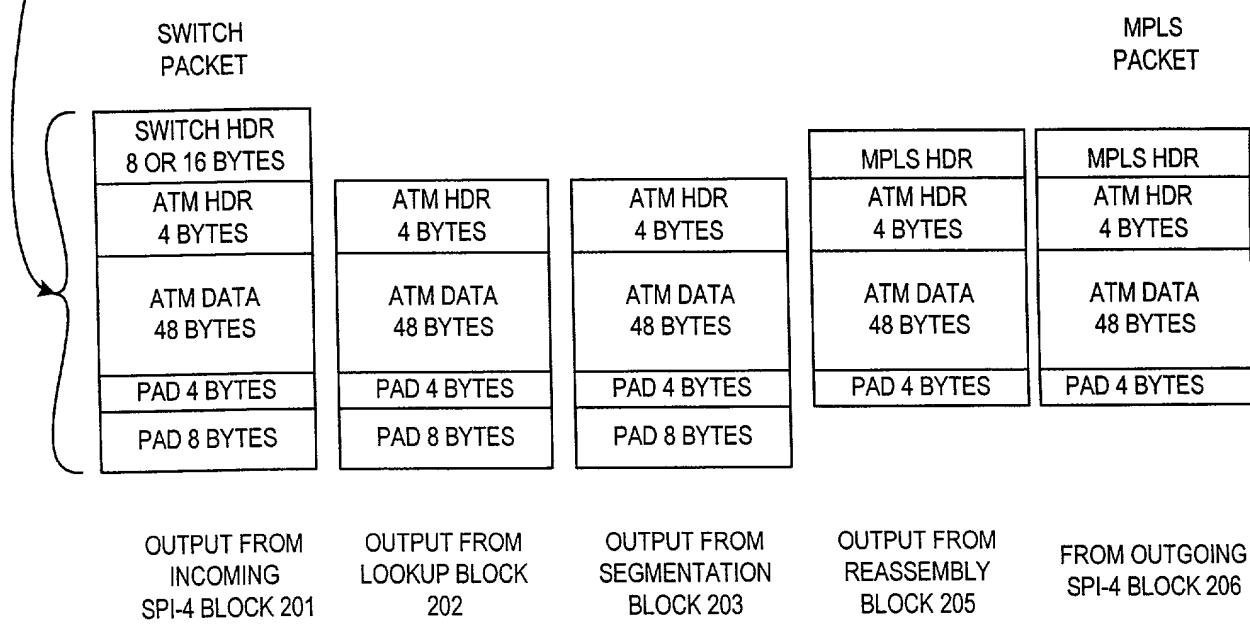
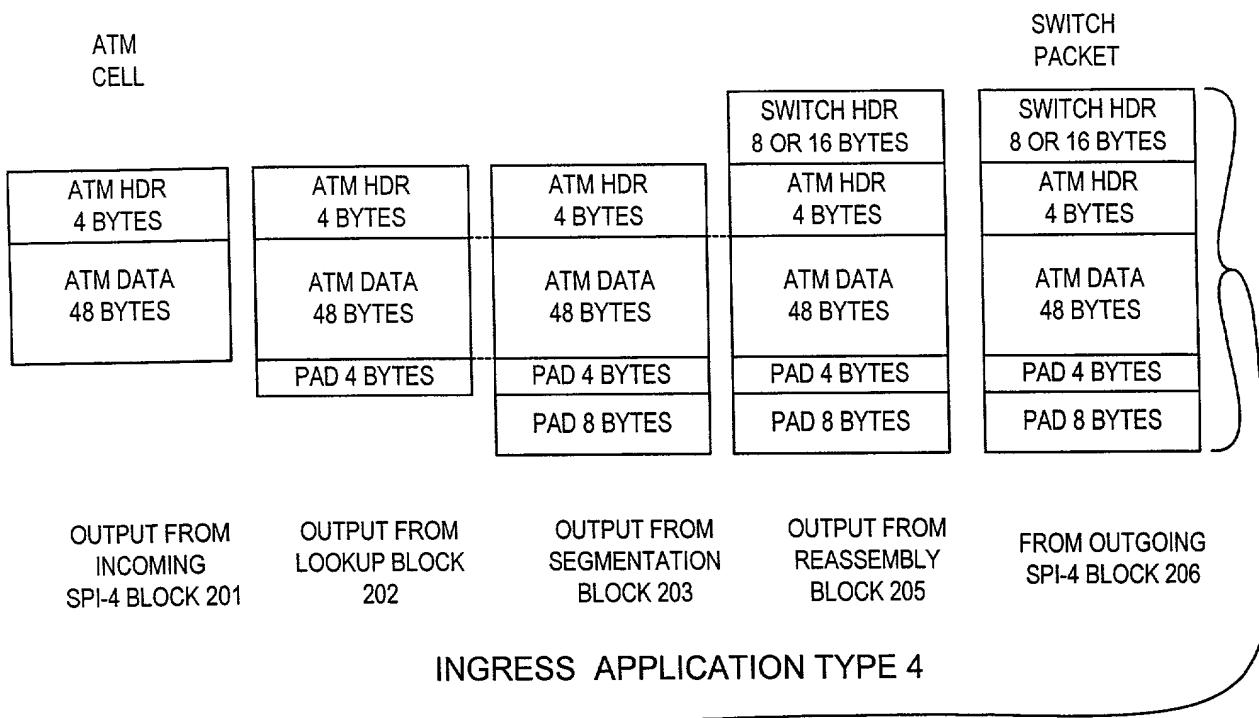


FIG. 44



EGRESS APPLICATION TYPE 14

FIG. 45

MPLS PACKET
(ATM CELL
ENCAPSULATED)

MPLS HDR
ATM HDR 4 BYTES
ATM DATA 48 BYTES

MPLS HDR
ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES

MPLS HDR
ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES
PAD 8 BYTES

MPLS HDR
ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES

SWITCH PACKET (ATM
CELL ENCAPSULATED)

SWITCH HDR 8 OR 16 BYTES
MPLS HDR
ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES

OUTPUT FROM
INCOMING
SPI-4 BLOCK 201

OUTPUT FROM
LOOKUP BLOCK
202

OUTPUT FROM
SEGMENTATION
BLOCK 203

OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206

INGRESS APPLICATION TYPE 6

SWITCH PACKET (ATM
CELL ENCAPSULATED)

SWITCH HDR 8 OR 16 BYTES
MPLS HDR
ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES

ATM
CELL

ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES

ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES
PAD 8 BYTES

ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES

ATM HDR 4 BYTES
ATM DATA 48 BYTES
PAD 4 BYTES

OUTPUT FROM
INCOMING
SPI-4 BLOCK 201

OUTPUT FROM
LOOKUP BLOCK
202

OUTPUT FROM
SEGMENTATION
BLOCK 203

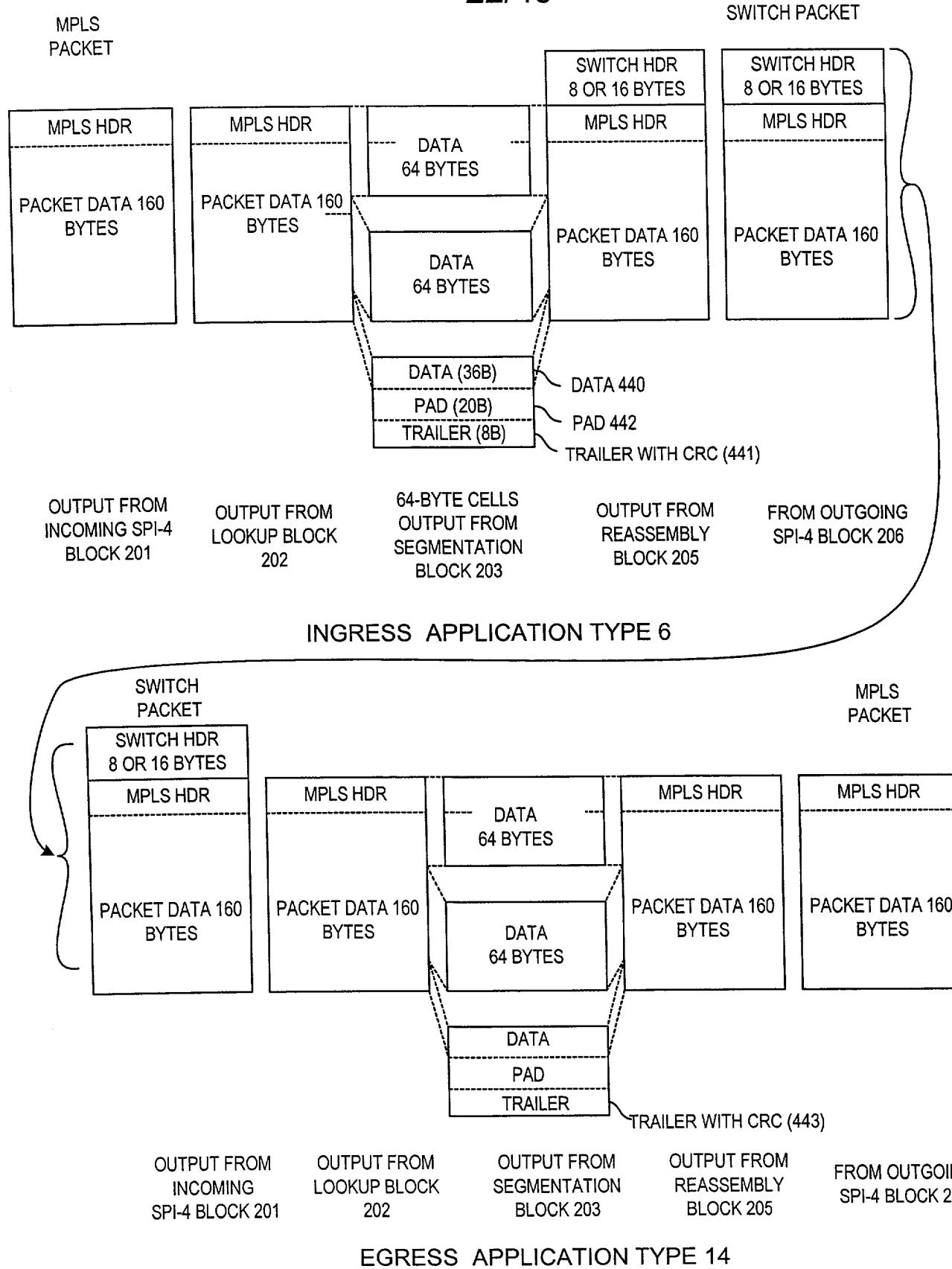
OUTPUT FROM
REASSEMBLY
BLOCK 205

FROM OUTGOING
SPI-4 BLOCK 206

EGRESS APPLICATION TYPE 12 (ATM DE-ENCAPSULATION)

FIG. 46

22/45

**FIG. 47**

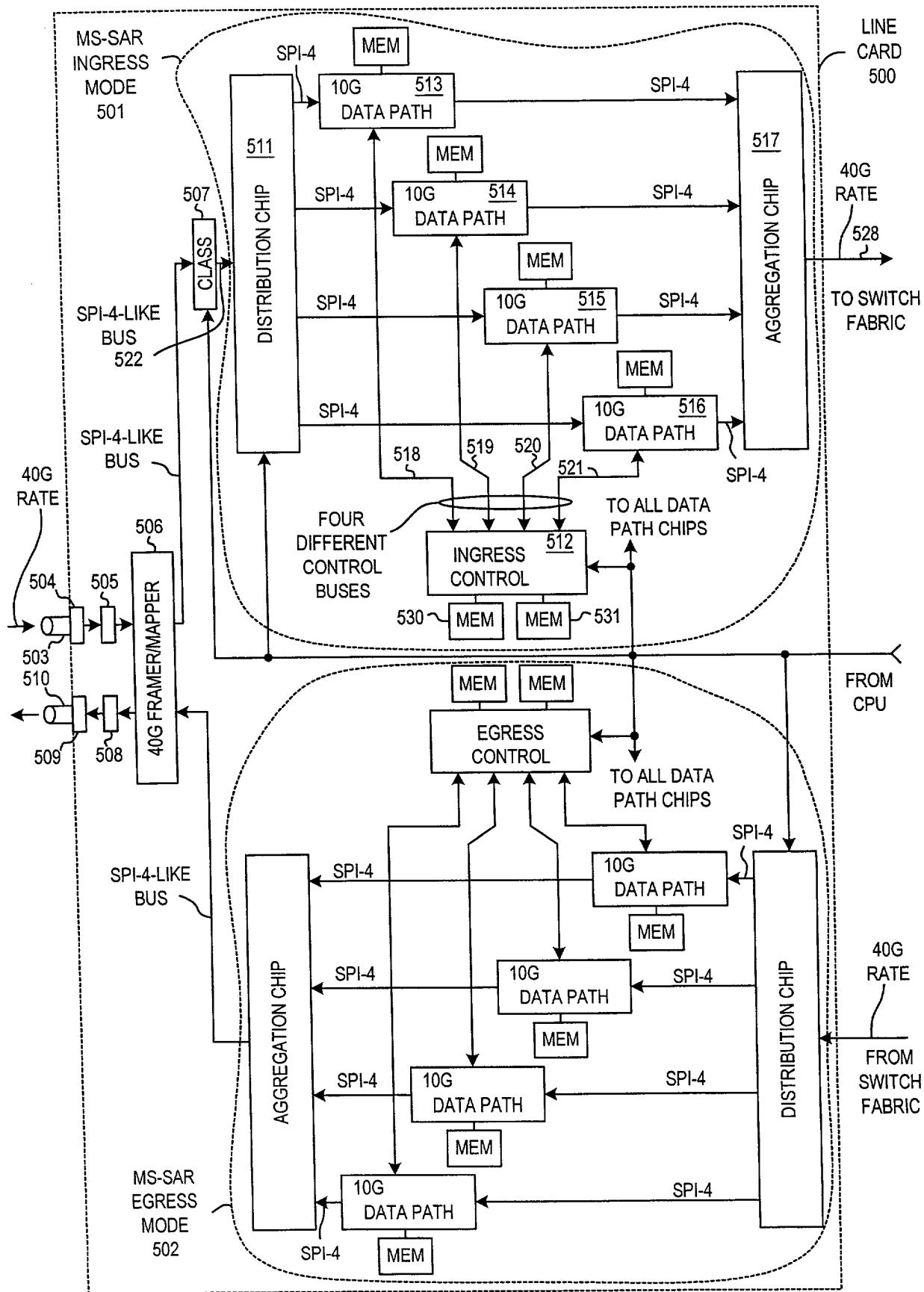


FIG. 48

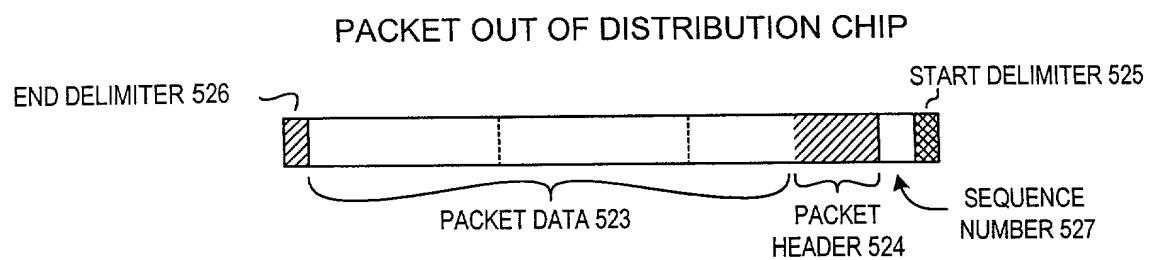
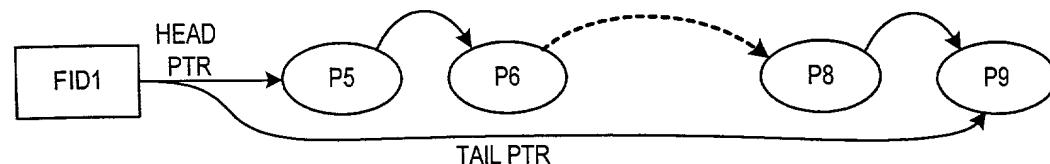
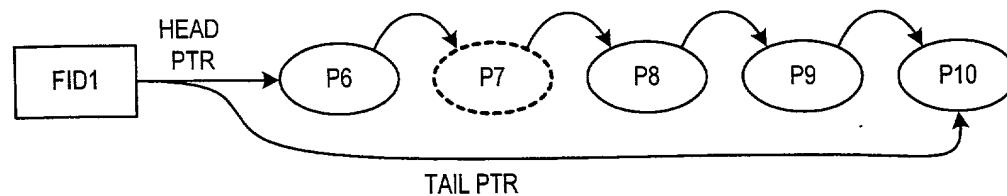


FIG. 49



PACKET QUEUE

FIG. 50



PACKET QUEUE

FIG. 51

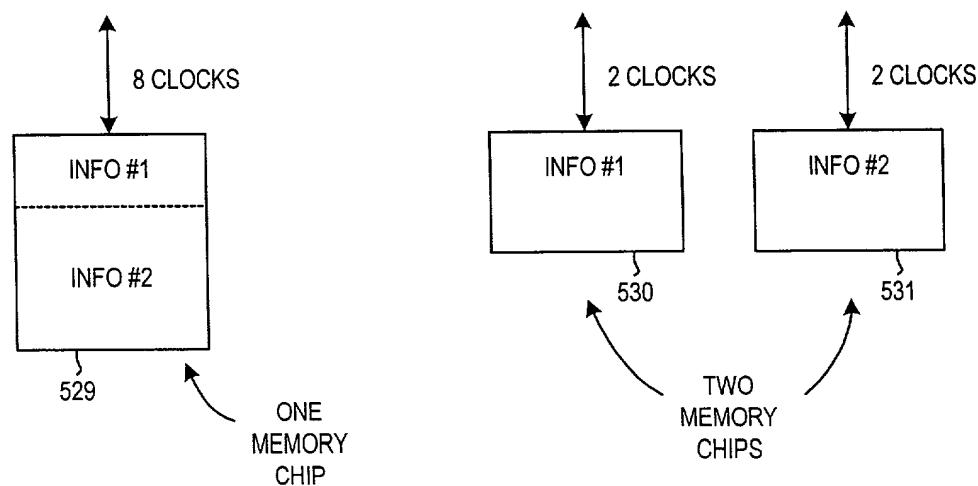


FIG. 52

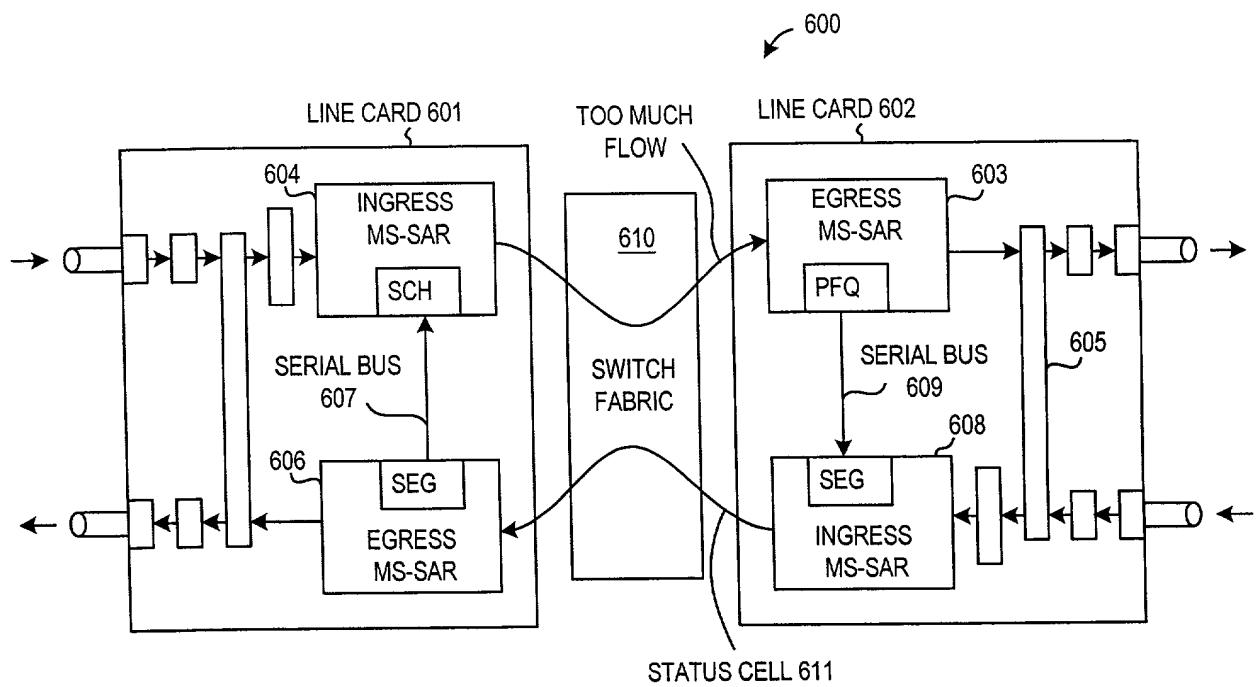
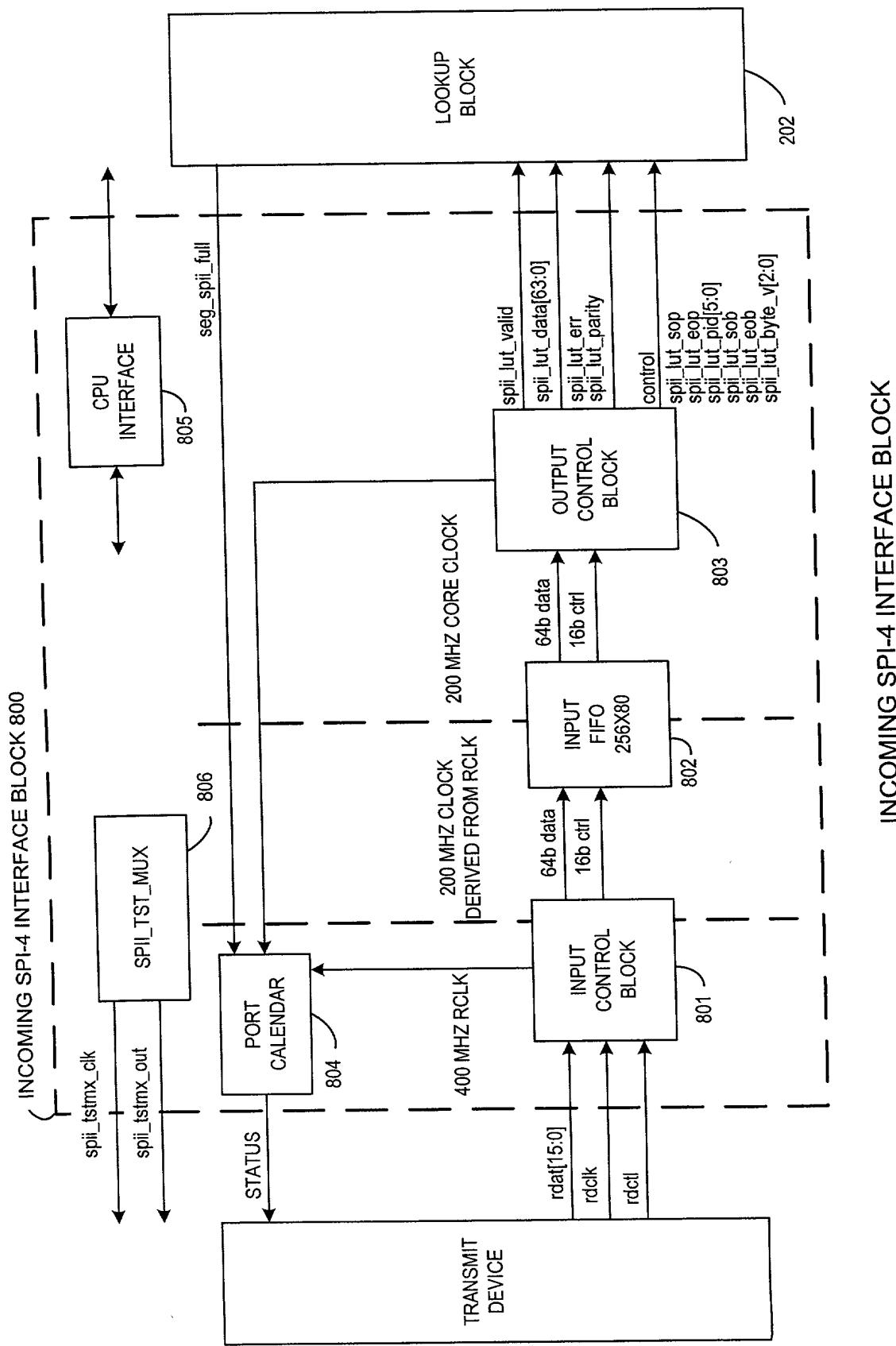
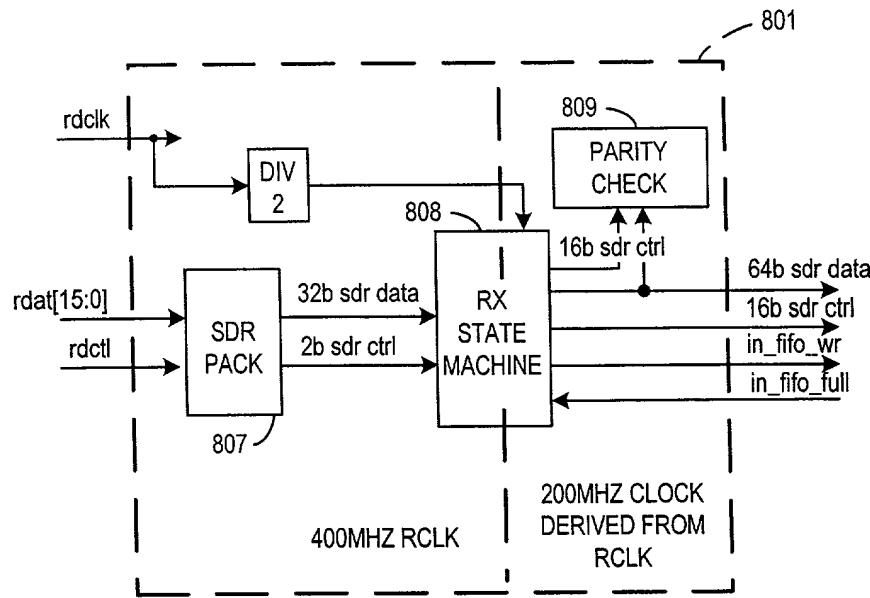
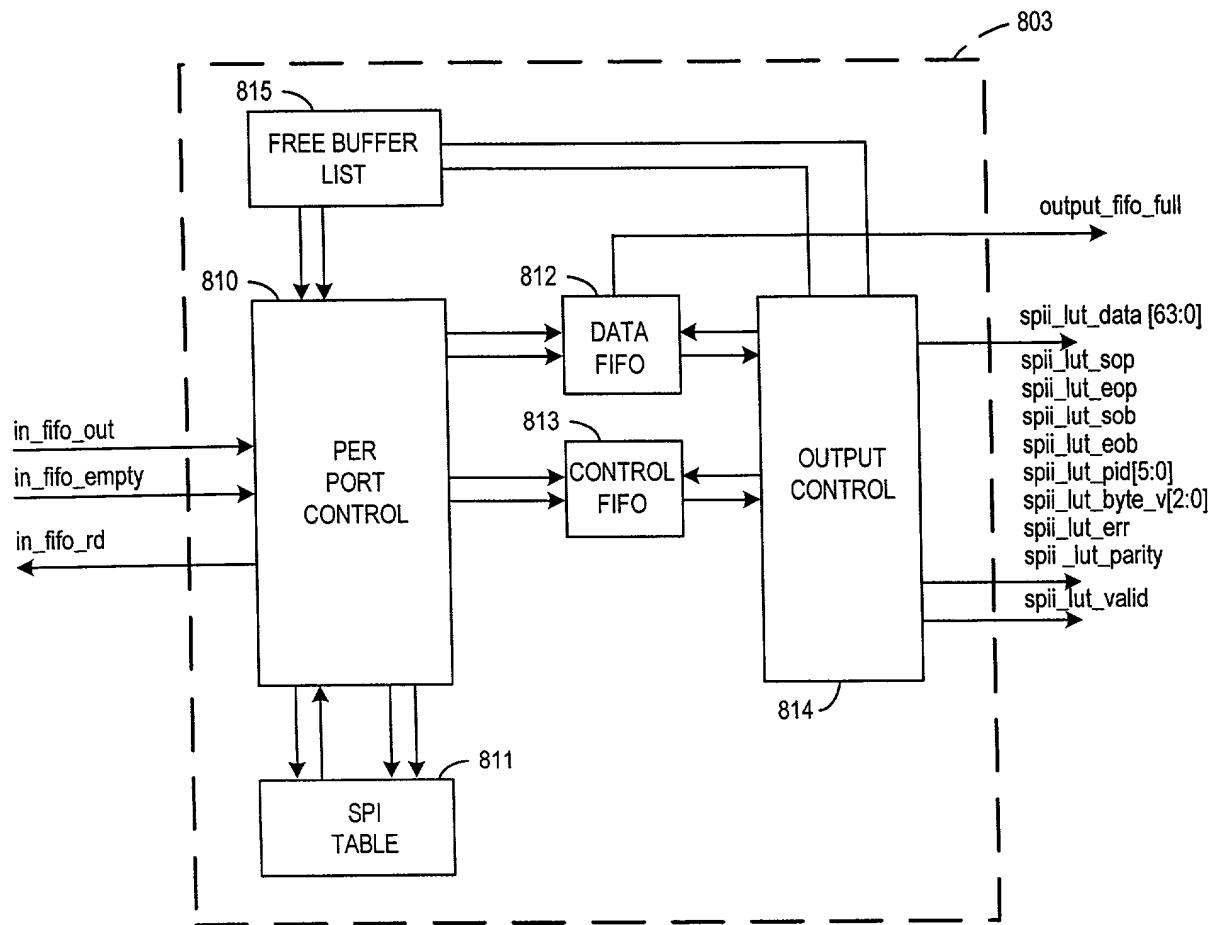


FIG. 53

**FIG. 54****INCOMING SPI-4 INTERFACE BLOCK**



INPUT CONTROL BLOCK

FIG. 55

OUTPUT CONTROL BLOCK

FIG. 56

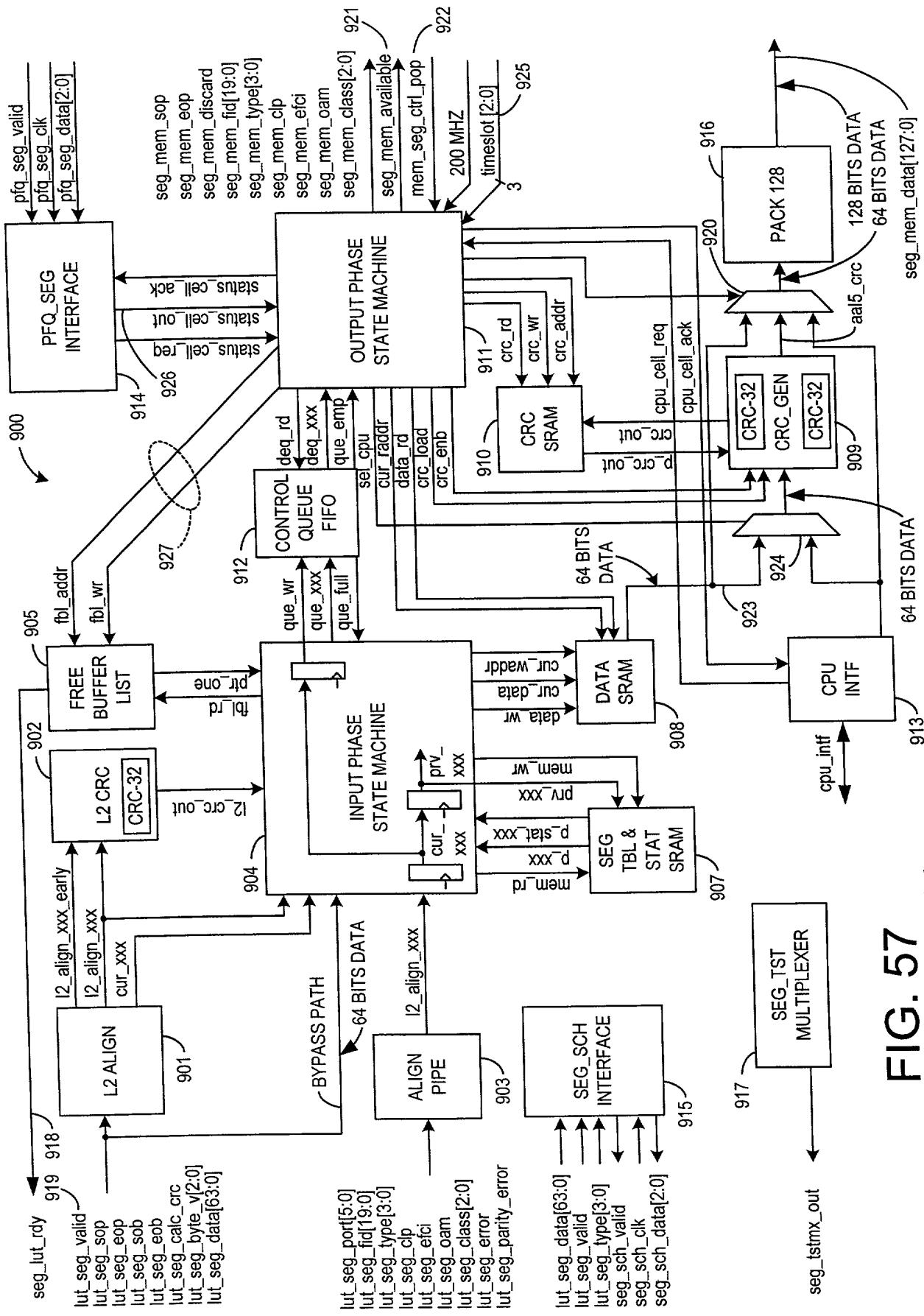


FIG. 57
SEGMENTATION BLOCK

**FIG. 58
MEMORY
MANAGER
BLOCK**

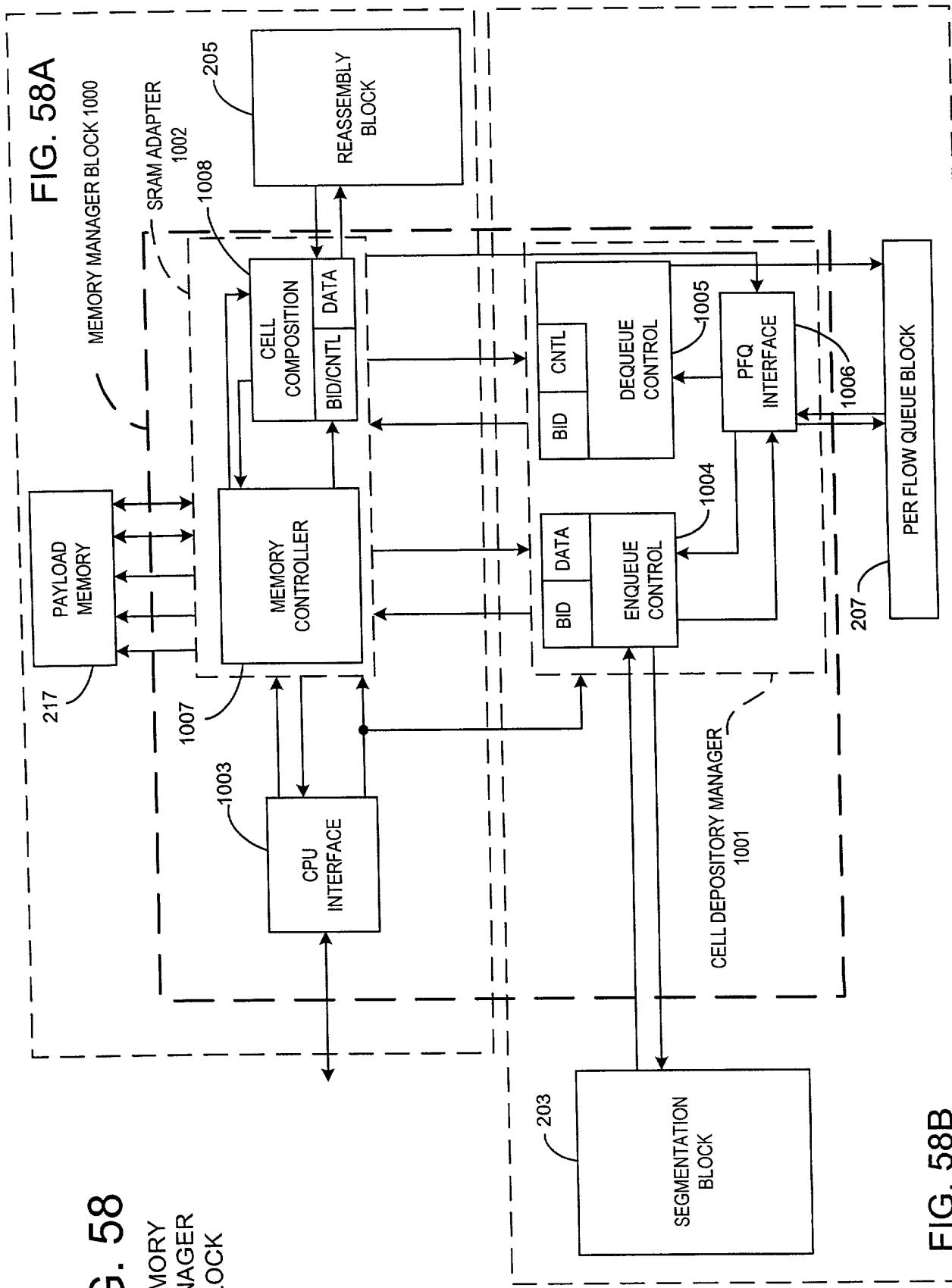
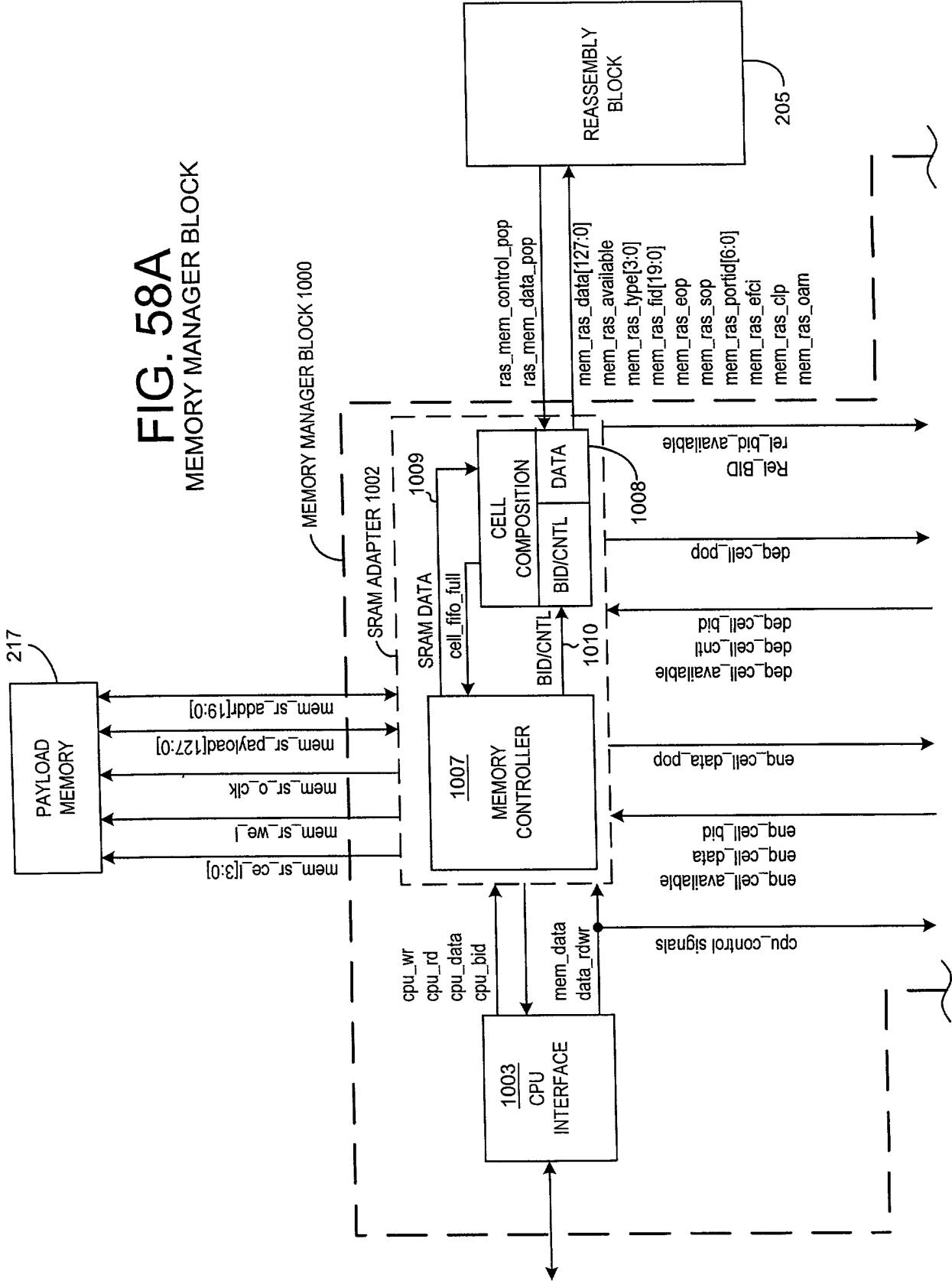


FIG. 58B

FIG. 58A
MEMORY MANAGER BLOCK



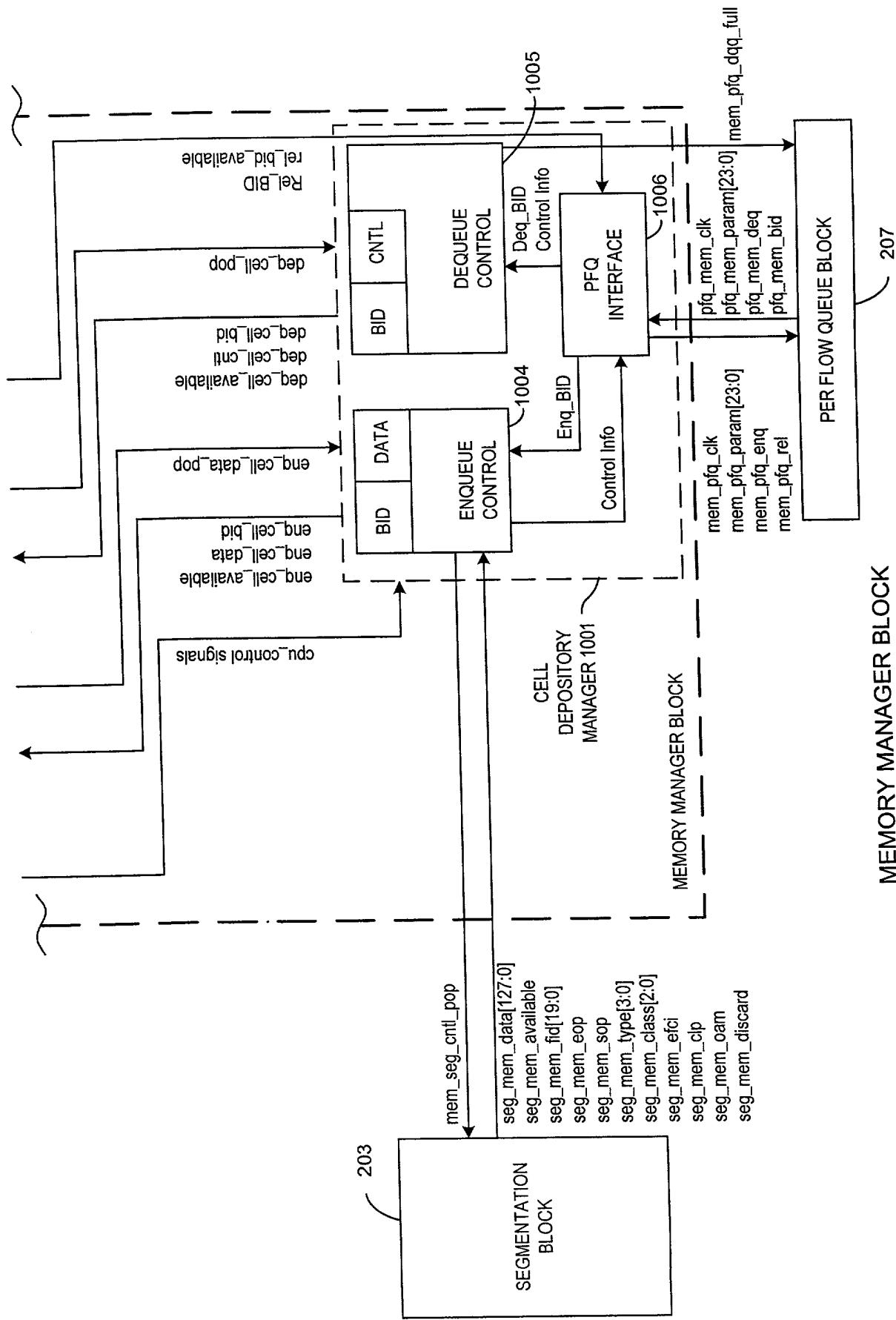


FIG. 58B

MEMORY MANAGER BLOCK

207

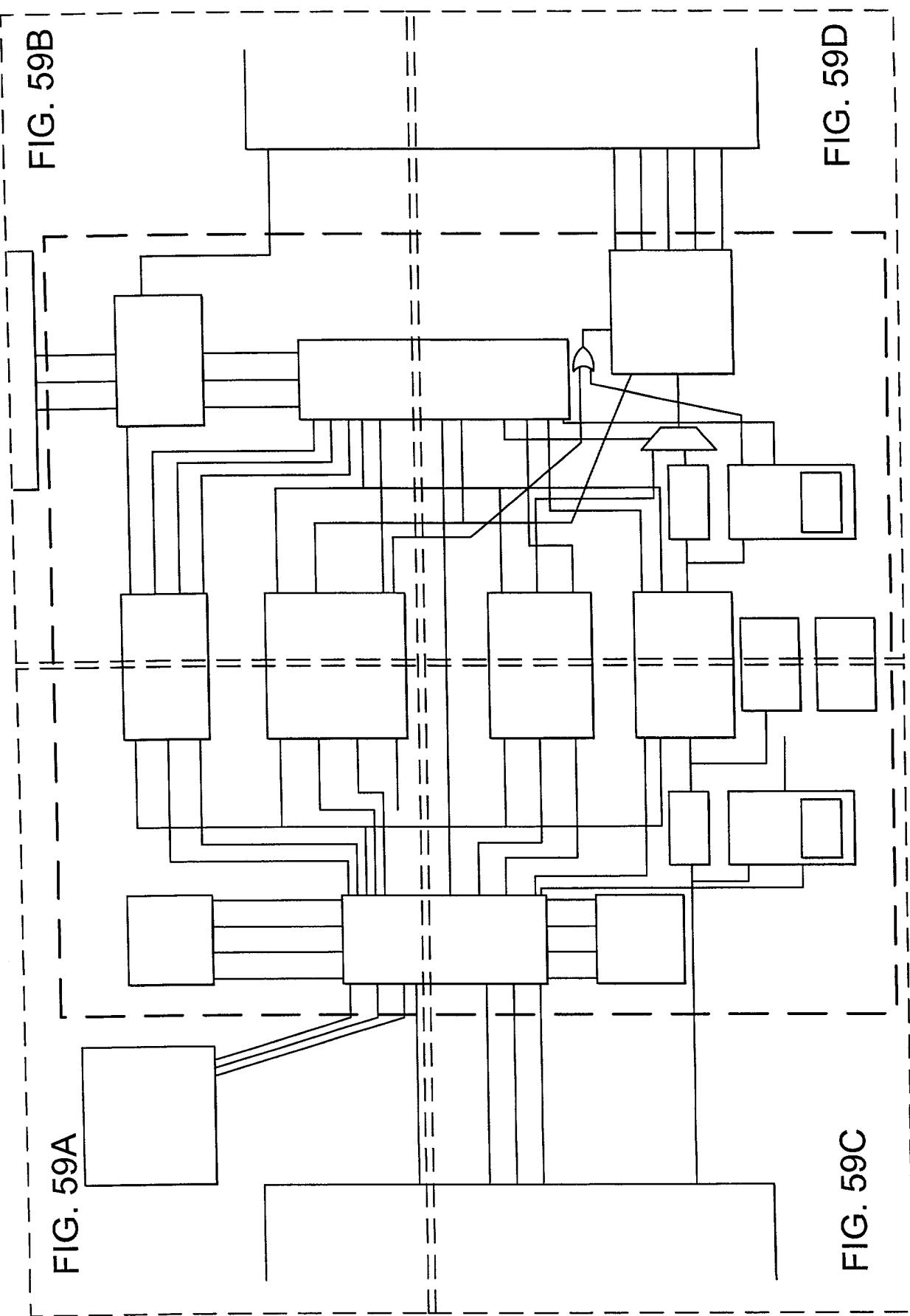


FIG. 59A

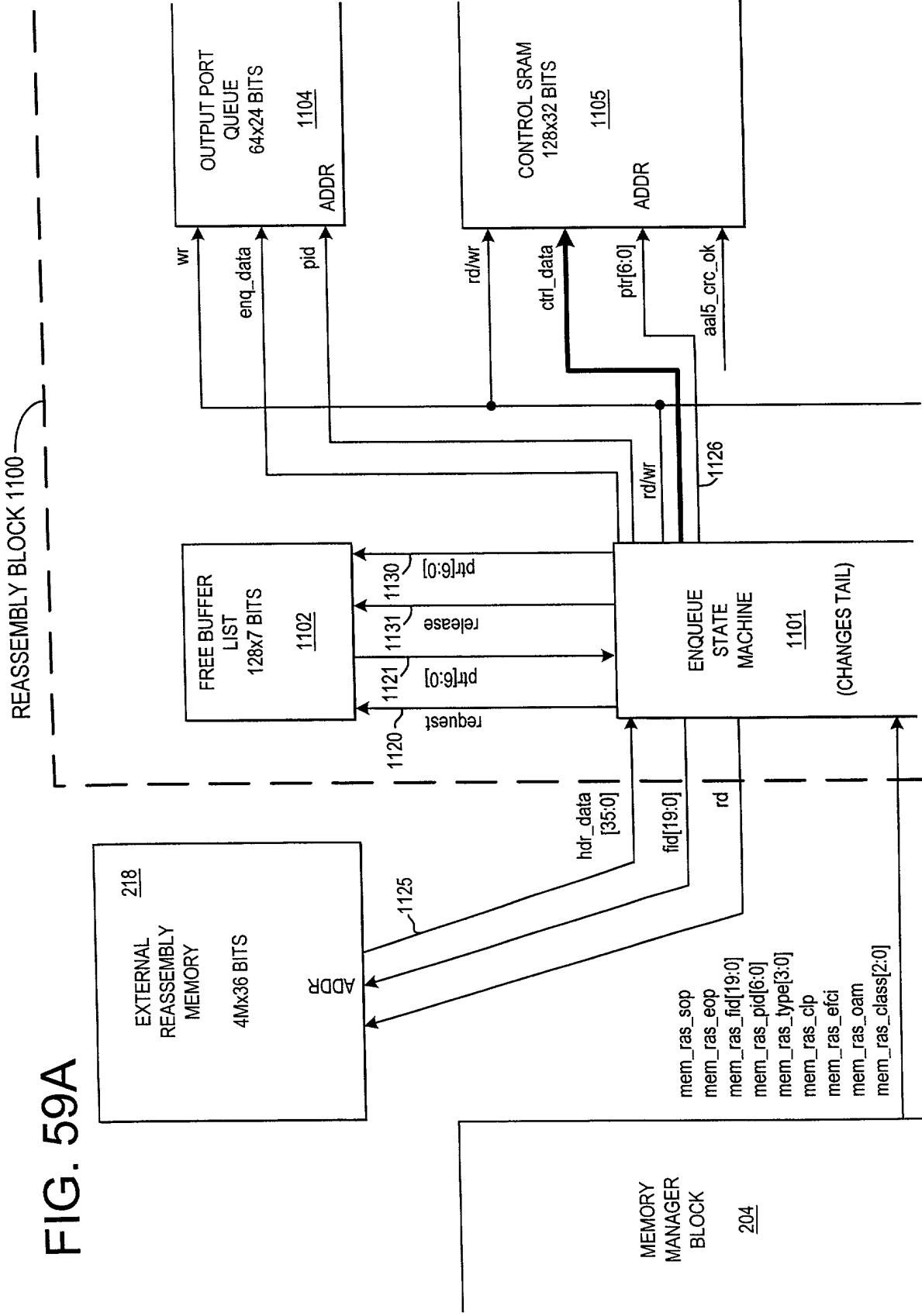
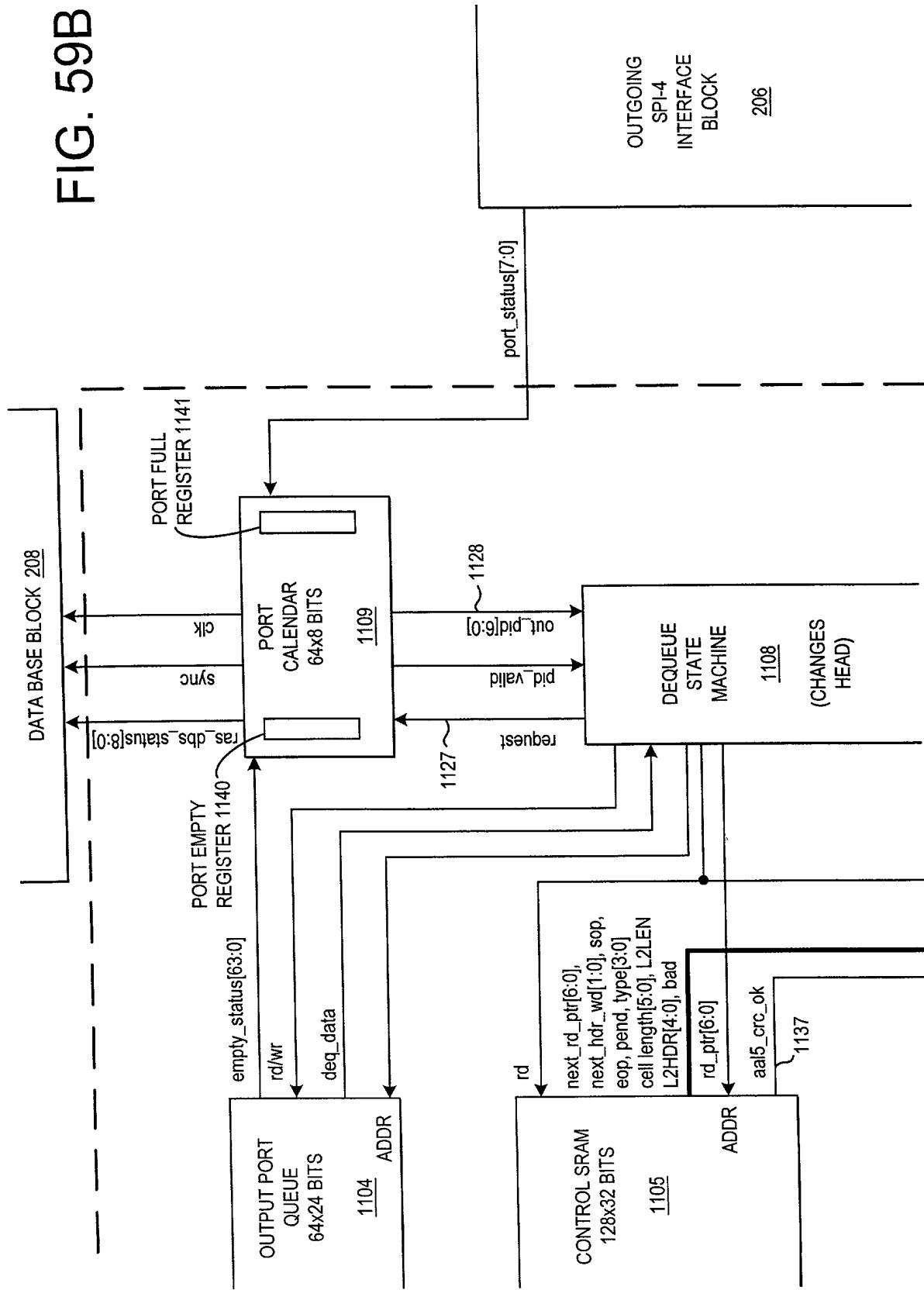


FIG. 59B



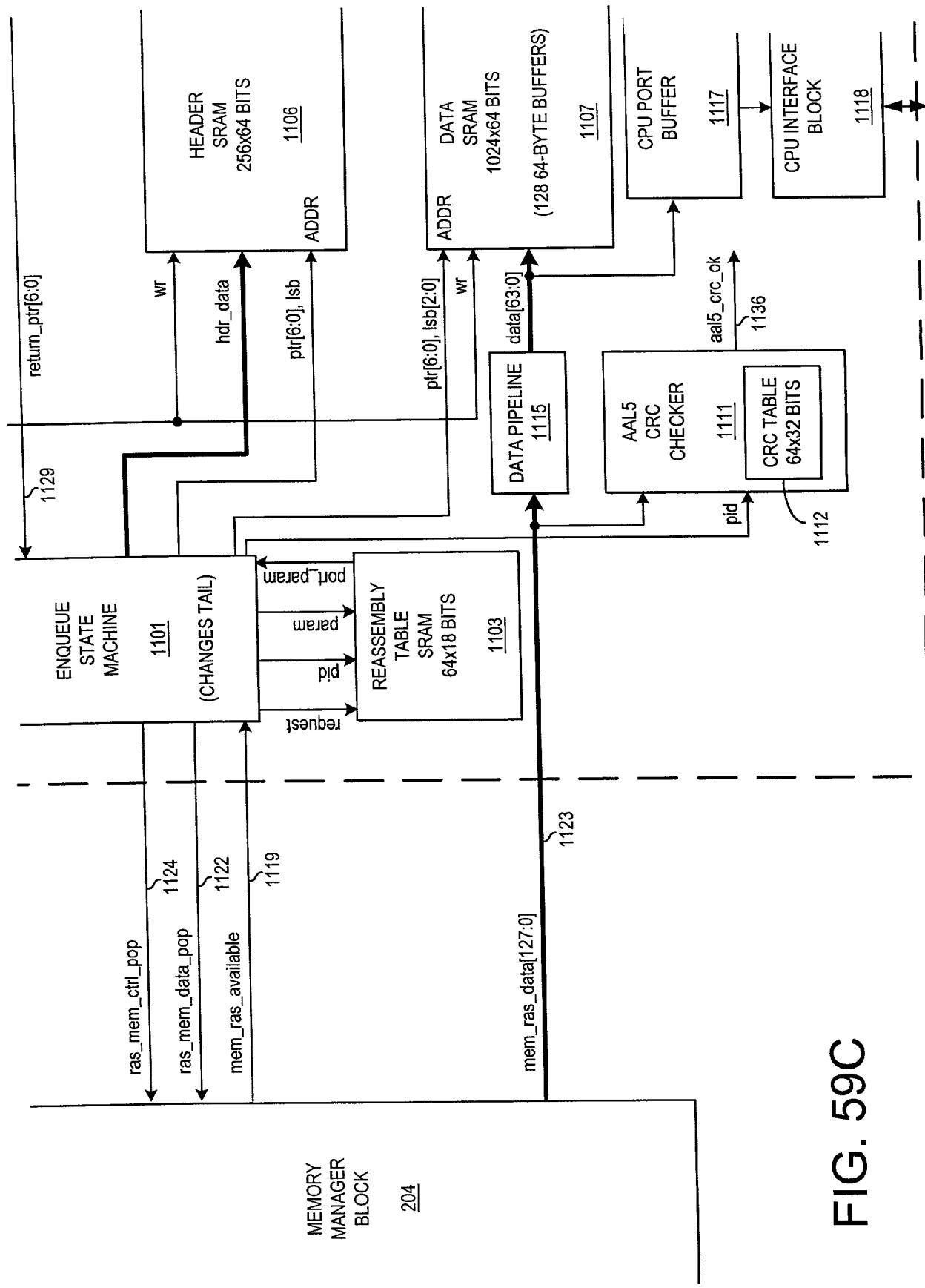


FIG. 59C

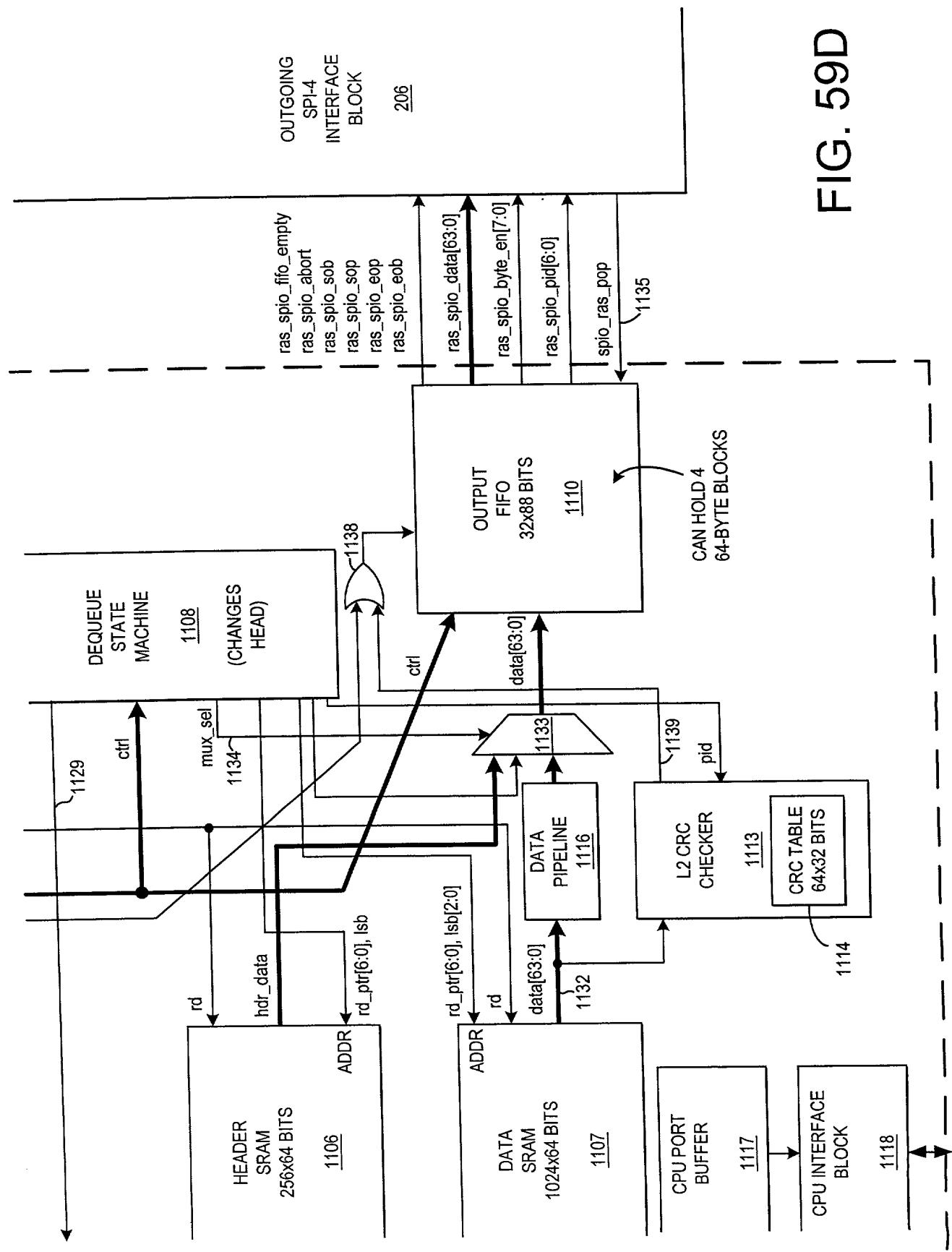


FIG. 59D

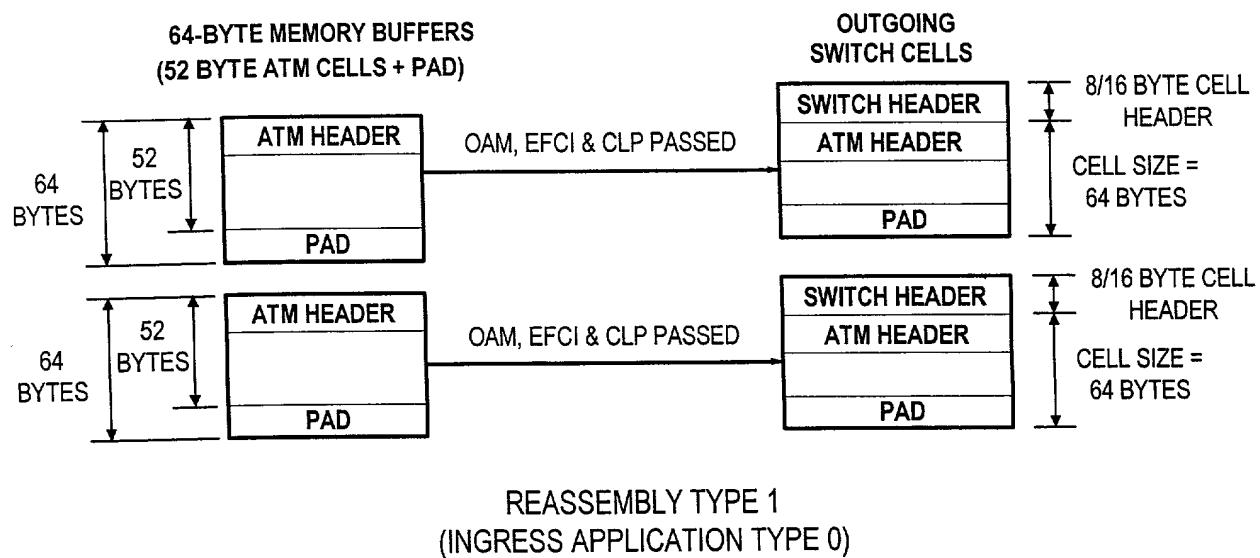


FIG. 60A

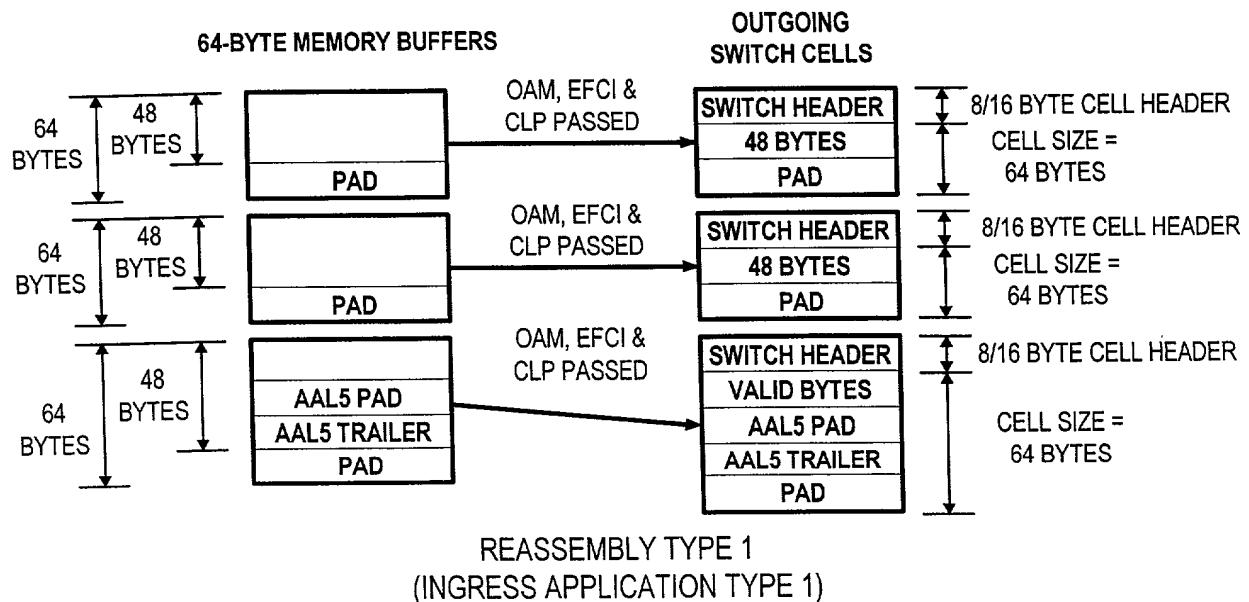
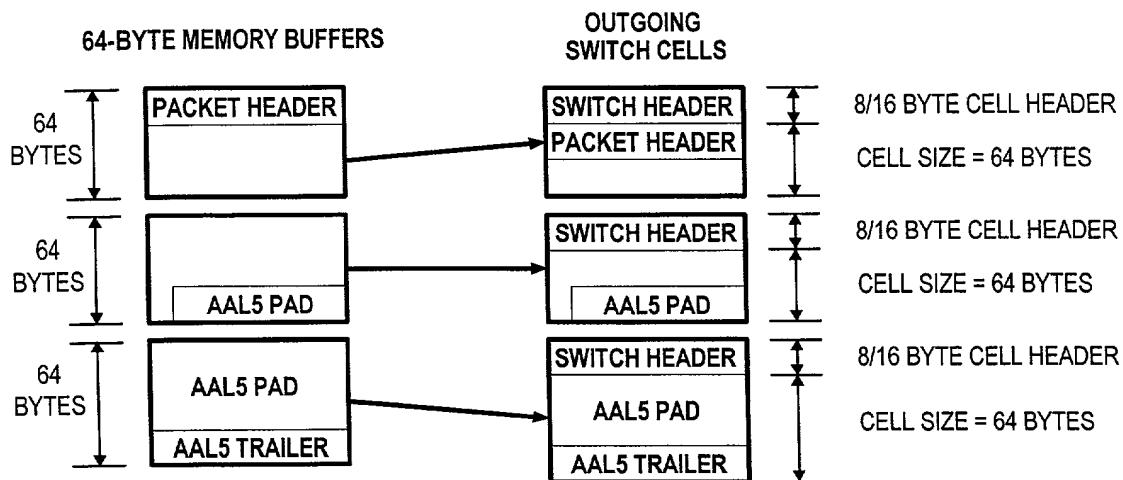
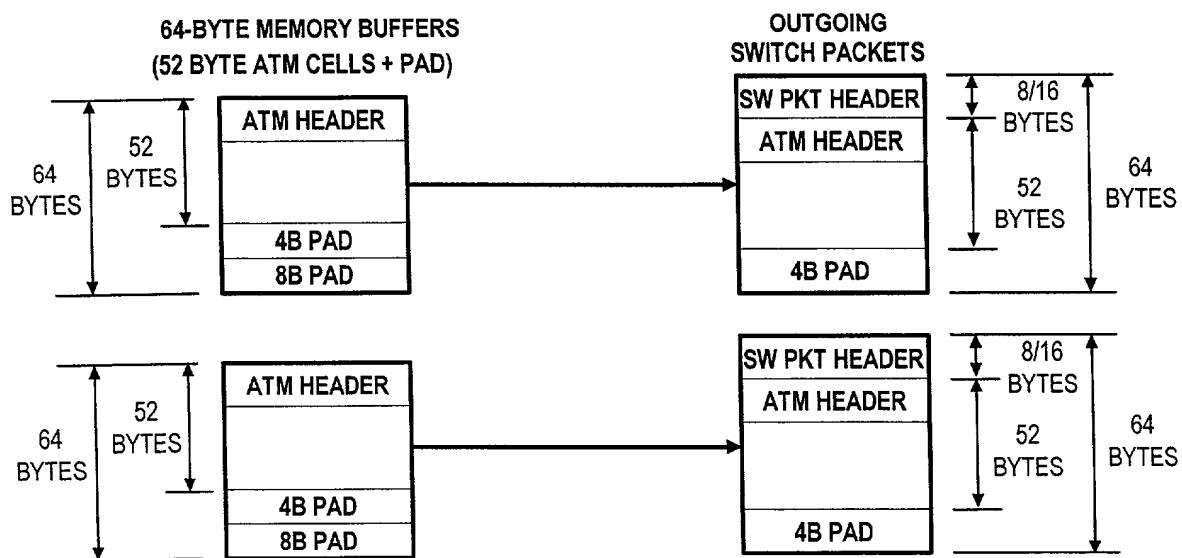


FIG. 60B



REASSEMBLY TYPE 1
(INGRESS APPLICATION TYPE 3)

FIG. 60C



REASSEMBLY TYPE 2
(INGRESS APPLICATION TYPE 4)

FIG. 60D

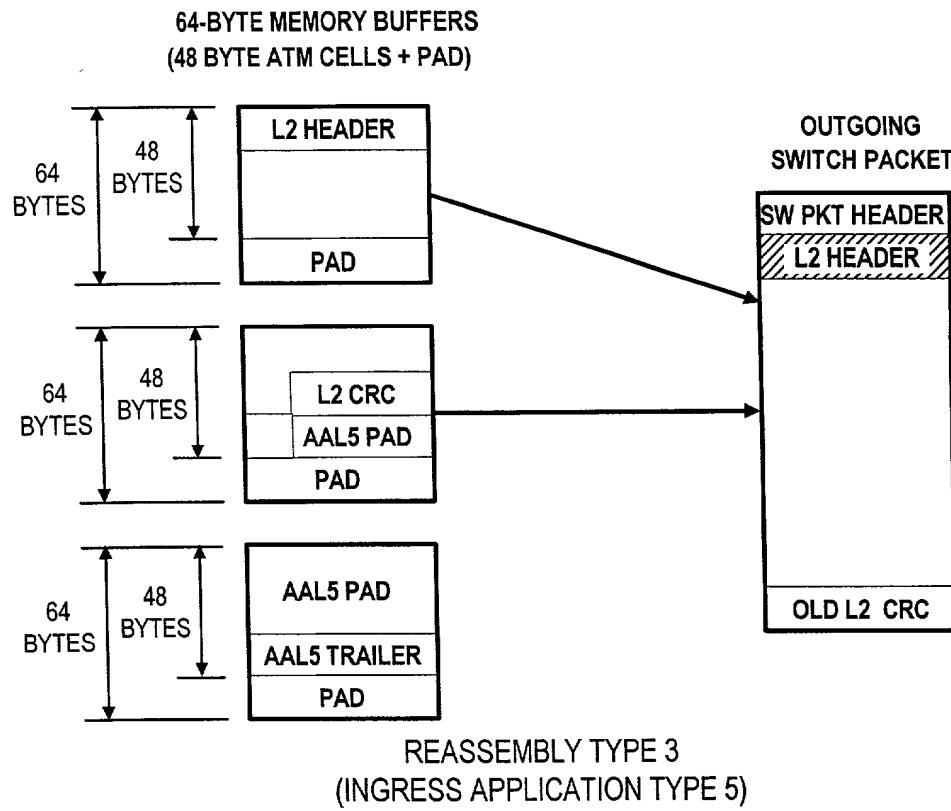


FIG. 60E

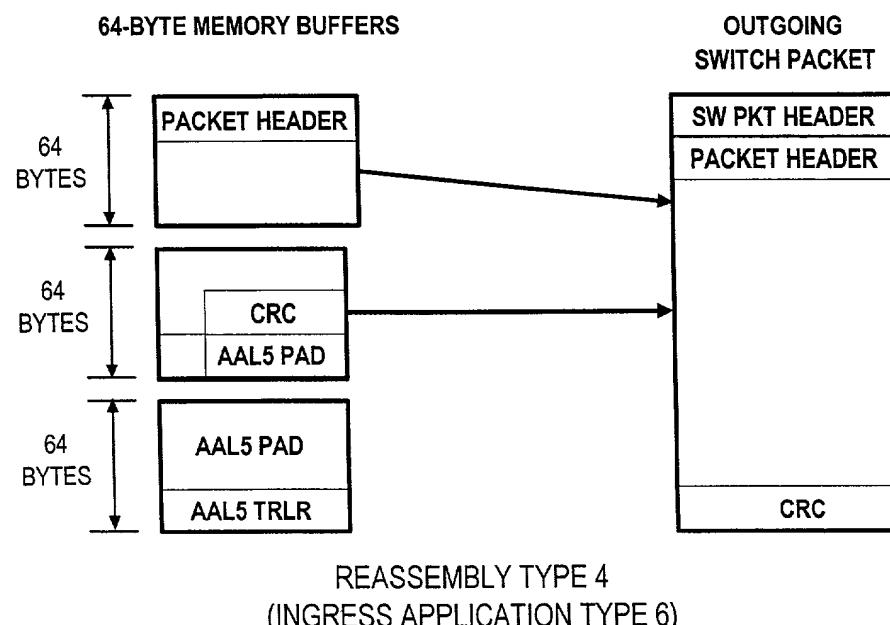
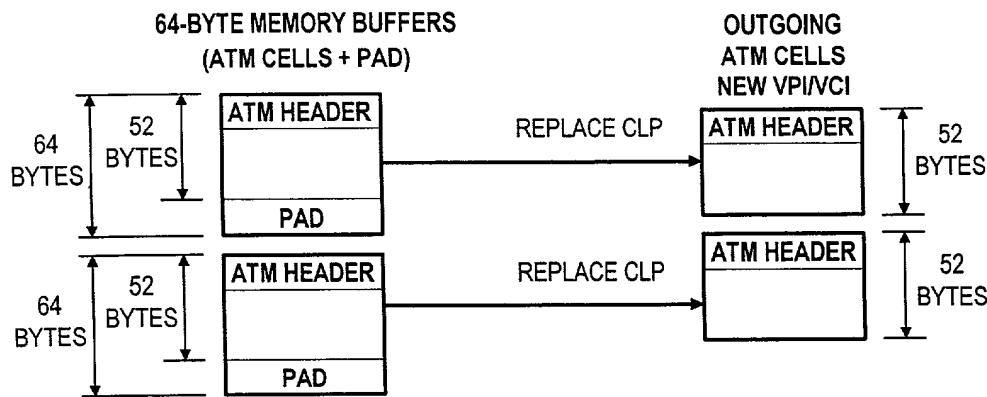
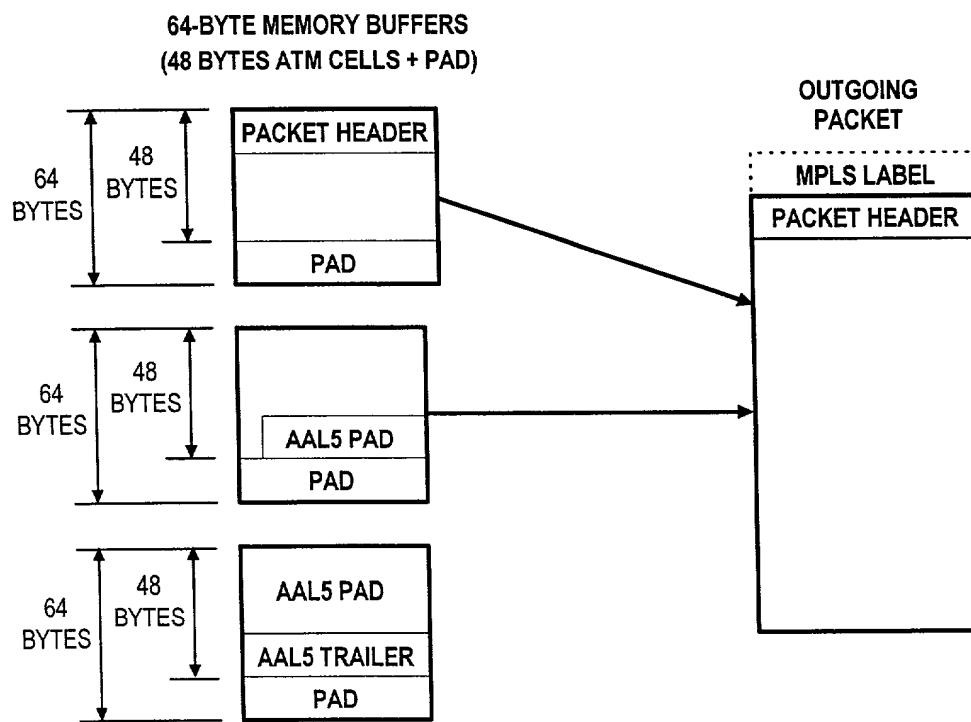


FIG. 60F



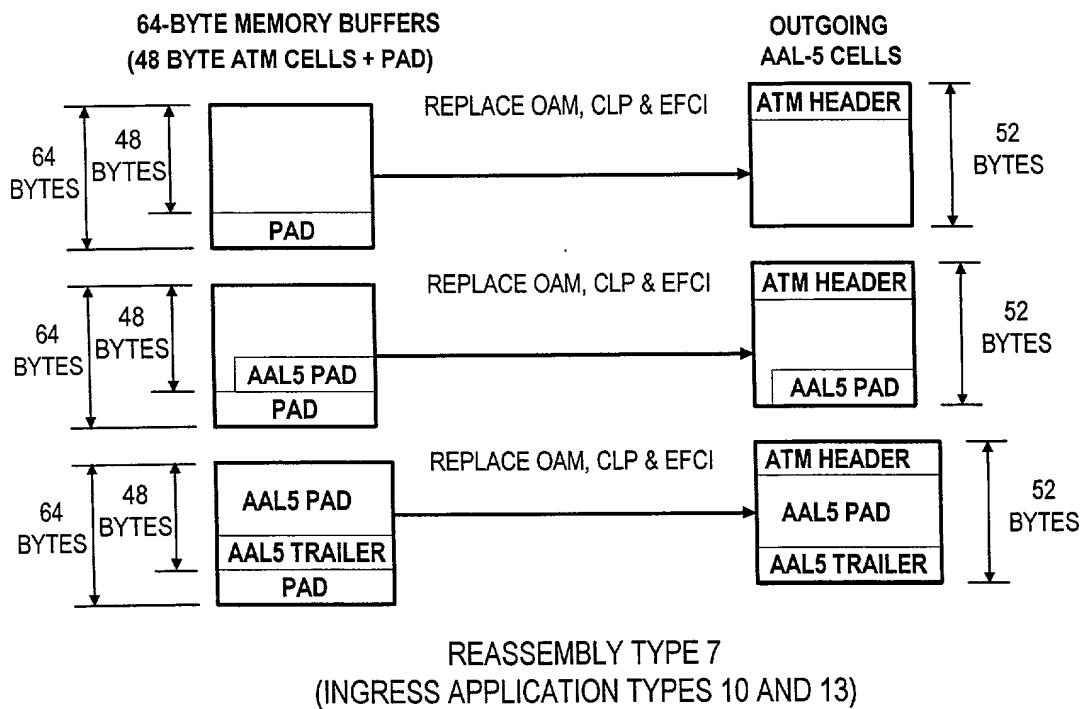
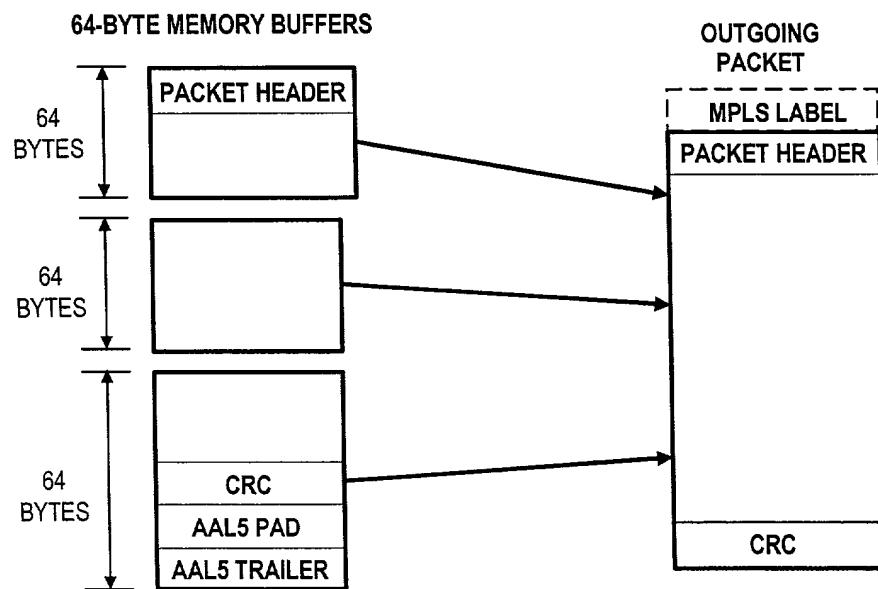
REASSEMBLY TYPE 5
(EGRESS APPLICATION TYPES 8 AND 12)

FIG. 60G



REASSEMBLY TYPE 6
(EGRESS APPLICATION TYPE 9)

FIG. 60H

**FIG. 60I****REASSEMBLY TYPE 8**
(INGRESS APPLICATION TYPES 11 AND 14)**FIG. 60J**

T. F. G. A. T. C. T. - S. I. D. E. E. Z. C. B. 6. 0

FIG. 61A

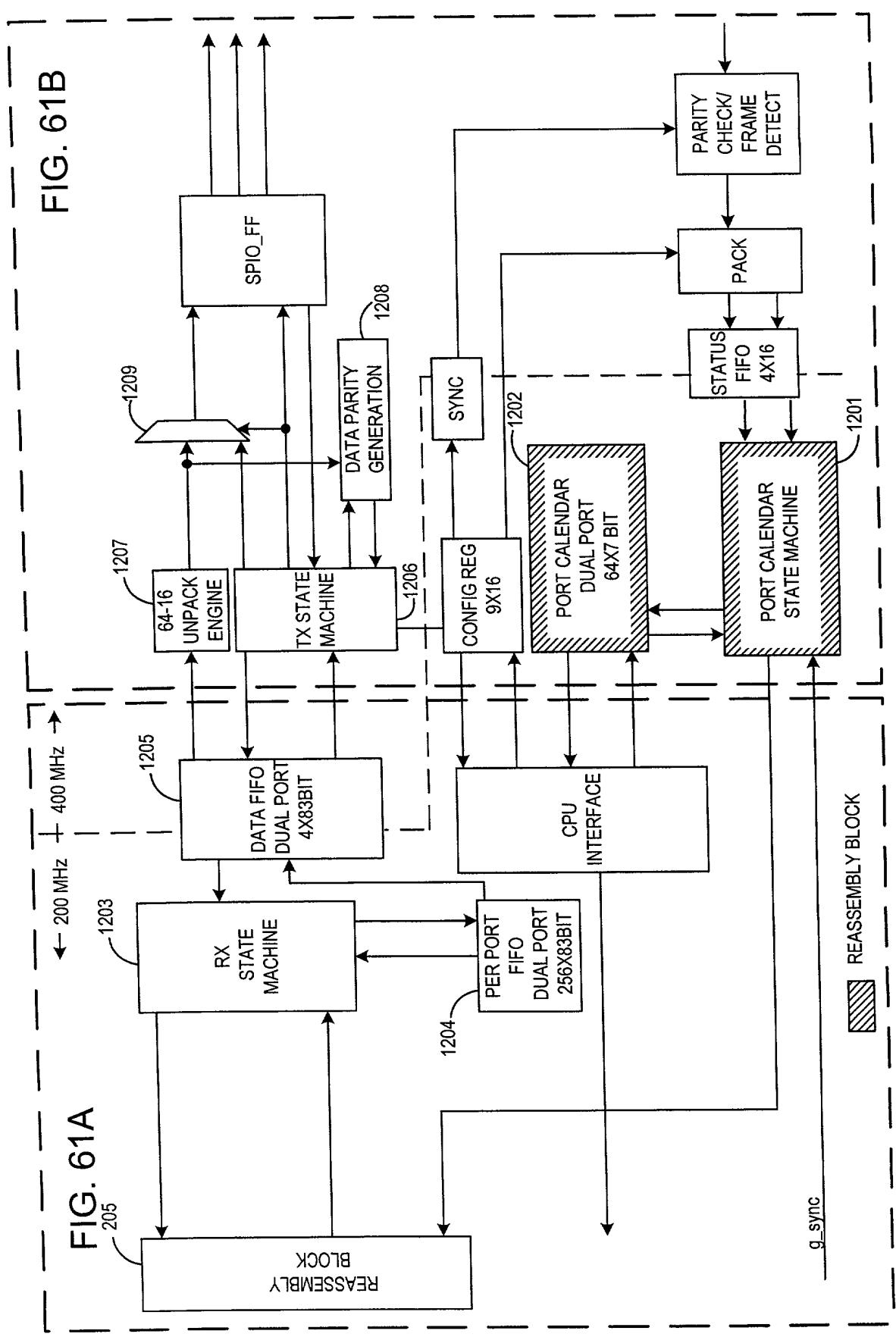
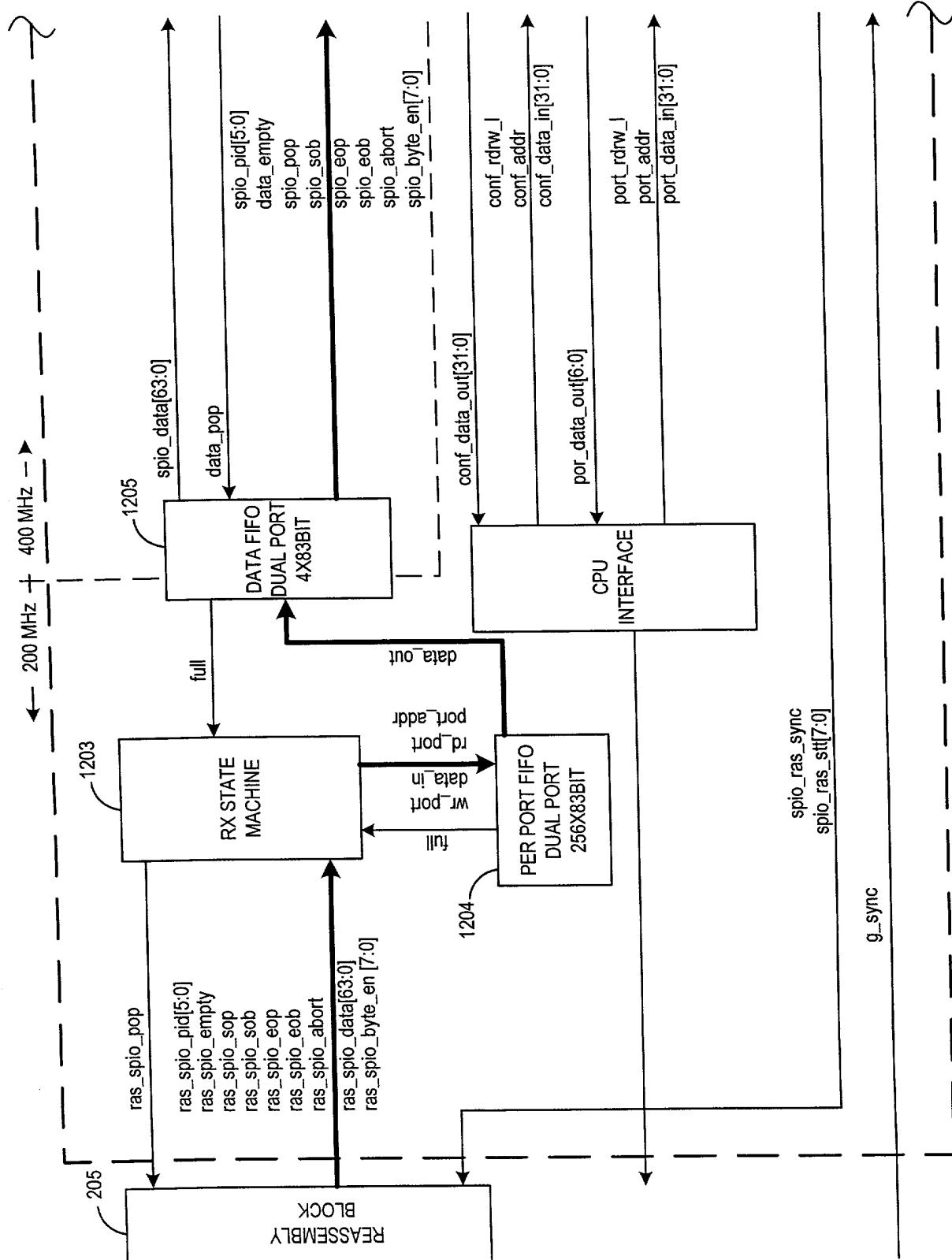


FIG. 61B

FIG. 61 OUTGOING SPI-4 INTERFACE BLOCK



OUTGOING SPI-4 INTERFACE BLOCK

FIG. 61A

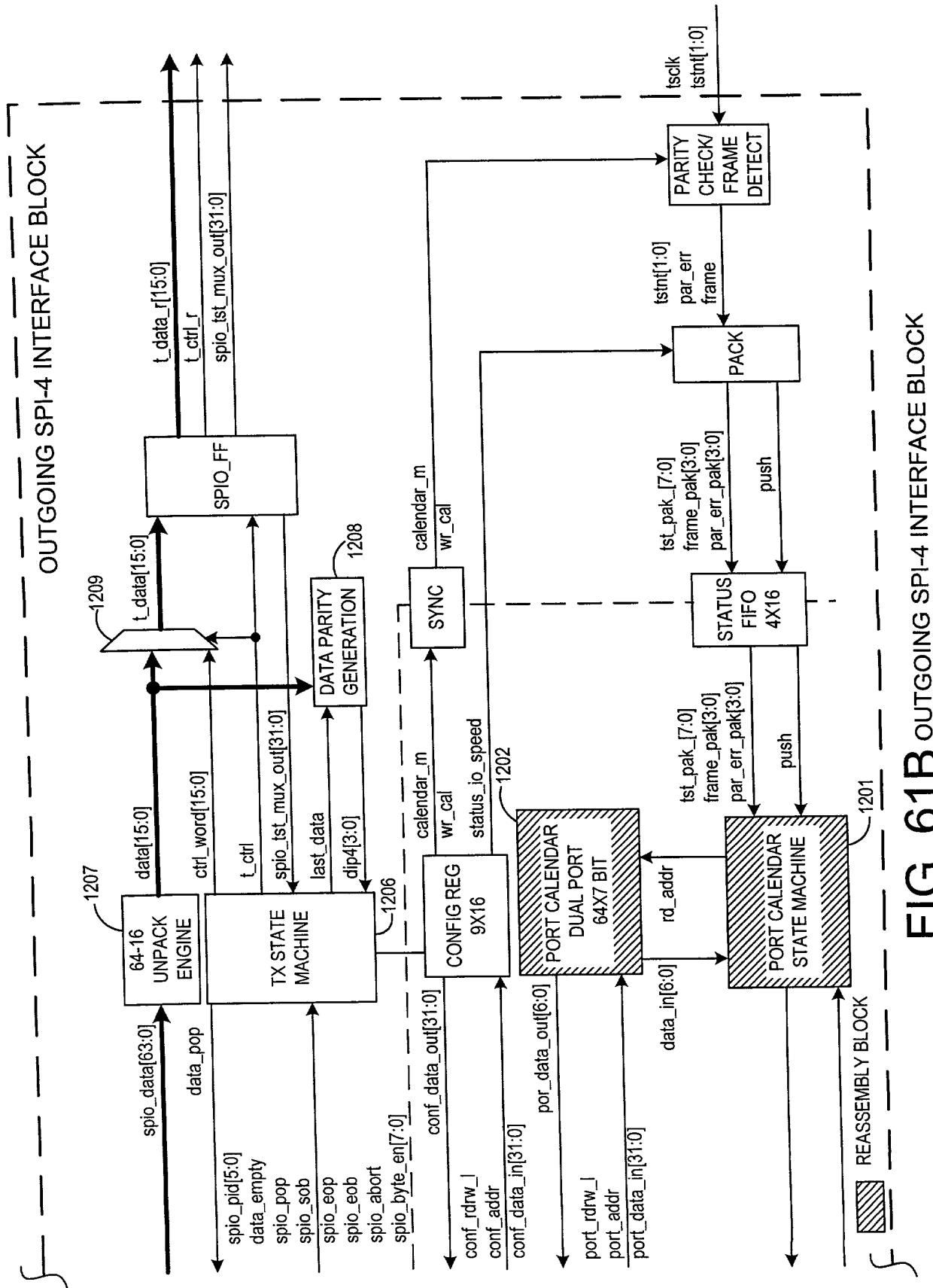


FIG. 61B OUTGOING SPI-4 INTERFACE BLOCK

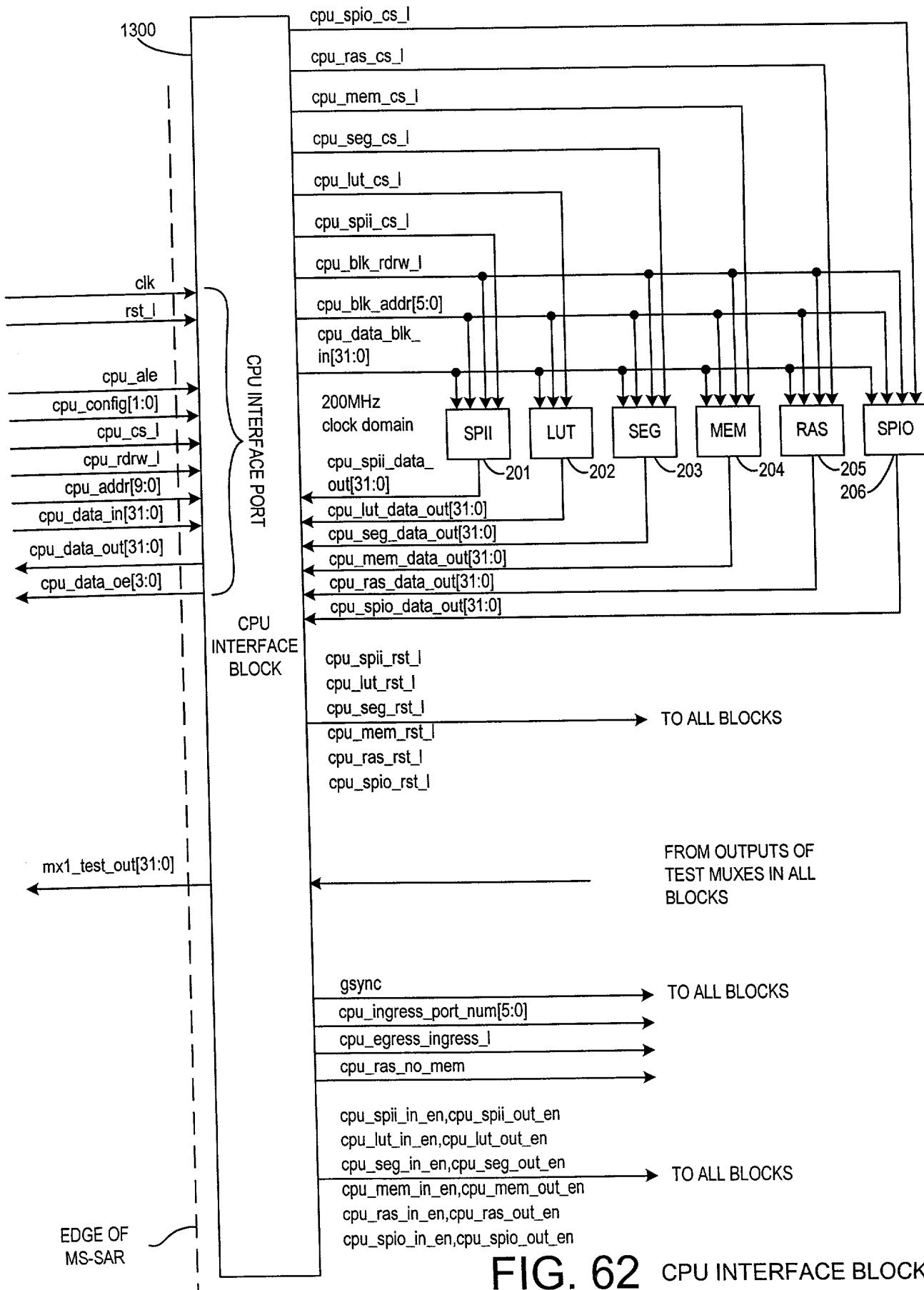


FIG. 62 CPU INTERFACE BLOCK